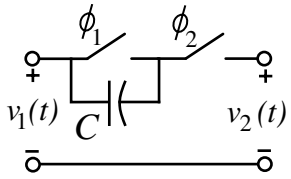
CHAPTER 9 – HOMEWORK SOLUTIONS

Problem 9.1-01

Develop the equivalent resistance expression in Table 9.1-1 for the series switched capacitor resistor emulation circuit.

Solution

The series switched capacitor is shown for reference purposes.



The average current flowing into the left-hand port can be written as,

$$i_1(average) = \frac{1}{T}\int_0^T i_1(t)dt = \frac{1}{T}\left(\int_0^{T/2} i_1(t)dt + \int_{T/2}^{T} i_1(t)dt\right)$$

or in terms of charge,

$$i_1(average) = \frac{1}{T}\int_0^{T/2} dq_1(t) + \frac{1}{T}\int_{T/2}^{T} dq_1(t) = \frac{q_1(T) - q_1(T/2)}{T}$$

By following through the sequence of switching, we see that,

$$q_1(T/2) = 0 \quad \text{and} \quad q_1(T) = C[v_1(T) - v_2(T)]$$

$$\therefore \qquad i_1(average) = \frac{C[v_1(T) - v_2(T)]}{T} \approx \frac{C[V_1 - V_2]}{T}$$

The average current of a series resistance, R, can be expressed as

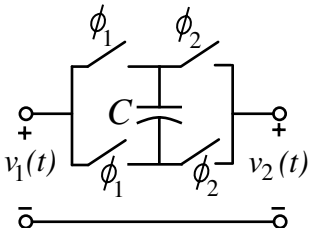
$$i_1(average) = \frac{[V_1 - V_2]}{R}$$

Equating the average currents gives

$$\boxed{R = \frac{T}{C}}$$

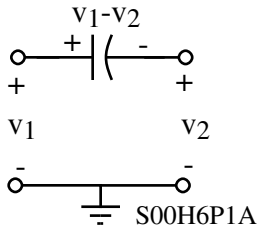
Problem 9.1-02

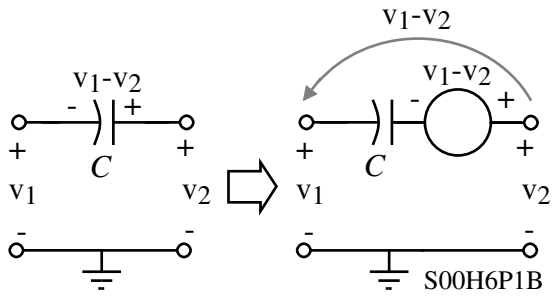
Develop the equivalent resistance expression for the bilinear switched capacitor resistor equivalent circuit shown below assuming that the clock frequency is much larger than the frequency of the signal.



Solution

ϕ_1 phase, $0<t<0.5T$: ϕ_2 phase, $0.5T<t<T$:





$$i_{Av} = \frac{1}{T}\int_0^T i(t)dt = \frac{2}{T}\int_{0.5T}^{T} i(t)dt = \frac{2}{T}\int_{0.5T}^{T} dq(t) = \frac{2}{T}2C(v_1\text{-}v_2) = \frac{4C}{T}(v_1\text{-}v_2)$$

$$\therefore\ R_{eq} = \frac{(v_1\text{-}v_2)}{i_{Av}} = \frac{T}{4C} \qquad \Rightarrow \qquad \boxed{R_{eq} = \frac{T}{4C}}$$

Problem 9.1-03

What is the accuracy of a time constant implemented with a resistor and capacitor having a tolerance of 10% and 5%, respectively. What is the accuracy of a time constant implemented by a switched capacitor resistor emulation and a capacitor if the tolerances of the capacitors are 5% and the relative tolerance is 0.5%. Assume that the clock frequency is perfectly accurate.

Solution

Continuous time accuracy:

$$\frac{d\tau_C}{\tau_C} = \frac{dR_1}{R_1} + \frac{dC_2}{C_2} = 10\%+5\% = \underline{\underline{15\%}}$$

Discrete-time accuracy:

$$\frac{d\tau_D}{\tau_D} = \frac{dC_2}{C_2} - \frac{dC_1}{C_1} - \frac{df_c}{f_c} = \underline{\underline{0.5\%}}$$

Problem 9.1-04

Repeat Example 9.1-3 using a series switched capacitor resistor emulation.

Solution

Problem 9.1-05

Find the z-domain transfer function for the circuit shown in Fig. 9.1-5. Let $\alpha = C_2/C_1$ and find an expression for the discrete time frequency response following the methods of Ex. 9.1-4. Design (find α) a first-order, highpass circuit having a -3dB frequency of 1kHz following the methods of Ex. 9.1-5. Assume that the clock frequency is 100kHz. Plot the frequency response for the resulting discrete time circuit and compare with a first-order, highpass, continuous time circuit.

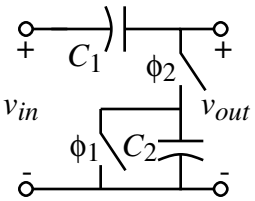


Figure P9.1-5

Solution

Problem 9.2-01

Fig. P9.2-1 shows two inverting summing amplifiers. Compare the closed-loop frequency response of these two summing amplifiers if the op amp is modeled by $A_{vd}(0) = 10{,}000$ and $GB = 1\text{MHz}$.

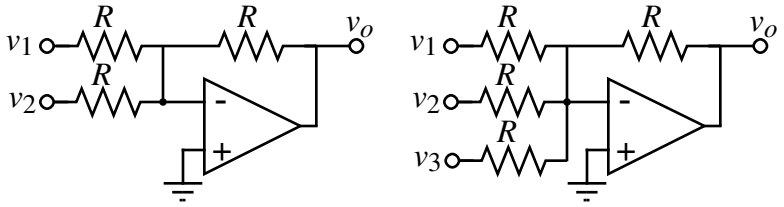


Figure P9.2-1 (a.) 2-input inverting summer. (b.) 3-input inverting summer.

Solution

A model for calculating the closed-loop frequency response is shown.

Solving for the output voltage,

$$V_{out} = -A\left(\frac{R}{(n+2)R}V_{out} + \frac{R}{(n+2)R}V_1\right)$$

$$V_{out}\left(1 + \frac{AR}{(n+2)R}\right) = -\frac{AR}{(n+2)R}V_1$$

$$\therefore \quad \frac{V_{out}}{V_1} = \frac{-\frac{A}{(n+2)}}{1 + \frac{A}{n+2}} = \frac{-\frac{1}{n+2}}{\frac{1}{A} + \frac{1}{n+2}} \quad \text{We know that } A(s) = \frac{A_{vd}(0)}{1 + \frac{s}{\omega_a}} \approx \frac{A_{vd}(0)\omega_a}{s} = \frac{GB}{s}$$

Substituting gives,

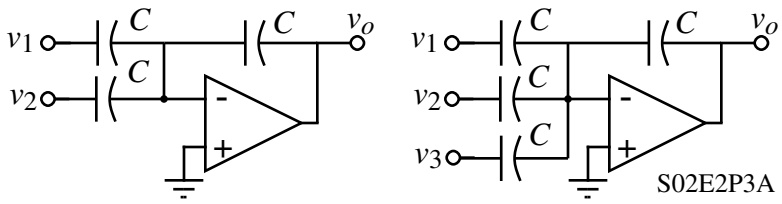
$$\frac{V_{out}}{V_1} = \frac{-\frac{1}{n+2}}{\frac{s}{GB} + \frac{1}{n+2}} = \frac{-\frac{GB}{n+2}}{s + \frac{GB}{n+2n}} = A_o\frac{\omega_{-3\text{dB}}}{s + \omega_{-3\text{dB}}}$$

$$\therefore \quad \omega_{-3\text{dB}} = \frac{GB}{n+2} \quad \text{and} \quad A_o = -1$$

For $n = 1$, $\underline{\underline{f_{-3\text{dB}} = GB/3 = 0.33\text{MHz}}}$ and for $n = 2$, $\underline{\underline{f_{-3\text{dB}} = GB/4 = 0.250\text{MHz}}}$

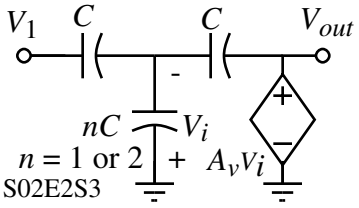
Problem 9.2-02

Two switched-capacitor summing amplifiers are shown. Find the value of the –3dB frequency of the closed-loop frequency response, v_o/v_1, with the remaining inputs shorted, of these two summing amplifiers if the op amp is modeled by $A_{vd}(0) = 10{,}000$ and $GB = 1\text{MHz}$.



Solution

A model for calculating the closed-loop frequency response is shown.



Solving for the output voltage,

$$V_{out} = -A\left(\frac{C}{(n+2)C}V_{out} + \frac{C}{(n+2)C}V_1\right)$$

$$V_{out}\left(1 + \frac{AC}{(n+2)C}\right) = -\frac{AC}{(n+2)C}V_1$$

$$\therefore \quad \frac{V_{out}}{V_1} = \frac{-\frac{A}{(n+2)}}{1 + \frac{A}{n+2}} = \frac{-\frac{1}{n+2}}{\frac{1}{A} + \frac{1}{n+2}} \quad \text{We know that } A(s) = \frac{A_{vd}(0)}{1 + \frac{s}{\omega_a}} \approx \frac{A_{vd}(0)\omega_a}{s} = \frac{GB}{s}$$

Substituting gives,

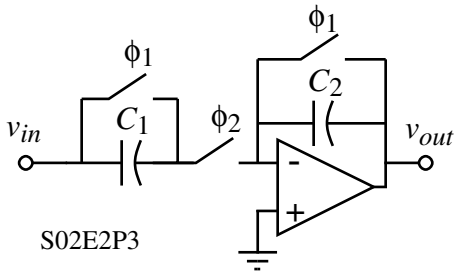
$$\frac{V_{out}}{V_1} = \frac{-\frac{1}{n+2}}{\frac{s}{GB} + \frac{1}{n+2}} = \frac{-\frac{GB}{n+2}}{s + \frac{GB}{n+2n}} = A_o\frac{\omega_{-3\text{dB}}}{s + \omega_{-3\text{dB}}}$$

$$\therefore \quad \omega_{-3\text{dB}} = \frac{GB}{n+2} \quad \text{and} \quad A_o = -1$$

For $n = 1$, $\underline{\underline{f_{-3\text{dB}} = GB/3 = 0.33\text{MHz}}}$ and for $n = 2$, $\underline{\underline{f_{-3\text{dB}} = GB/4 = 0.250\text{MHz}}}$

Problem 9.2-03

Find the z-domain transfer function for $H^{ee}(z)$ for the switched capacitor circuit shown.



Solution

In phase ϕ_2, the circuit is simply a charge amplifier whose transfer function is given as

$$H^{ee}(z) = \frac{V^{e}_{out}(z)}{V^{e}_{in}(z)} = -\frac{C_1}{C_2}$$

Problem 9.2-04

Verify the transresistance of Fig. 9.2-6a.

Solution

Positive transresistance realization:

$$R_T = \frac{v_1(t)}{i_2(t)} = \frac{v_1}{i_2(average)}$$

If we assume $v_1(t)$ is ≈ constant over one period of the clock, then we can write

$$i_2(average) = \frac{1}{T}\int_{T/2}^{T} i_2(t)dt = \frac{q_2(T) - q_2(T/2)}{T} = \frac{Cv_C(T) - Cv_C(T/2)}{T} = \frac{Cv_1}{T}$$

Substituting this expression into the one above shows that $\boxed{R_T = T/C}$

Problem 9.2-05

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oe}(z)$. (2.) If $C_1 = 10C_2$, plot the magnitude and phase response of the switched capacitor circuit from 0 Hz to the clock frequency (f_c). Assume that the op amp is ideal for this problem.

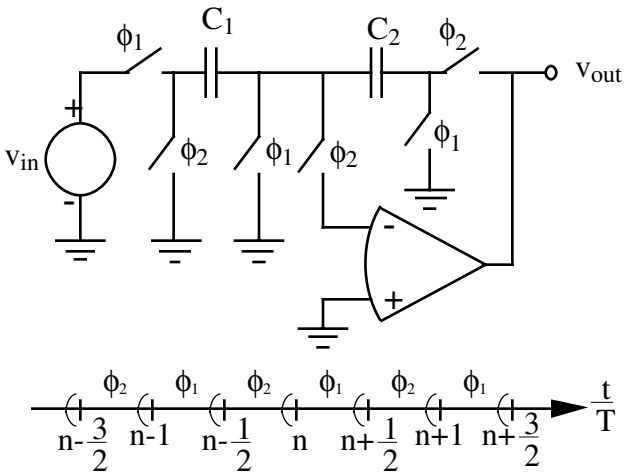


Figure P9.2-5

Solution

(1.) This circuit is a noninverting amplifier with a minimum number of switches.

ϕ_1: $t = (n\text{-}1)T$

$$v_{C1}^{o}(n\text{-}1) = v_{in}^{o}(n\text{-}1) \quad \text{and} \quad v_{C2}^{o}(n\text{-}1) = 0$$

ϕ_2: $t = (n\text{-}0.5)T$

$$v_{out}^{e}(n\text{-}0.5) = -\frac{C_1}{C_2}\left[-v_{in}^{o}(n\text{-}1)\right] = \frac{C_1}{C_2}v_{in}^{o}(n\text{-}1)$$

$$\therefore \quad V_{out}^{e}(z) = \frac{C_1}{C_2}z^{-1/2}\,v_{in}^{o}(z) \quad \rightarrow \quad H^{oe}(z) = \frac{C_1}{C_2}z^{-1/2} = \underline{\underline{10z^{-1/2}}}$$

(2.) $H^{oe}(e^{j\omega T}) = 10e^{-j\omega T/2} = 10e^{-j2\pi f/2f_c} = 10e^{-j\pi f/f_c}$

Plotting this transfer function gives,

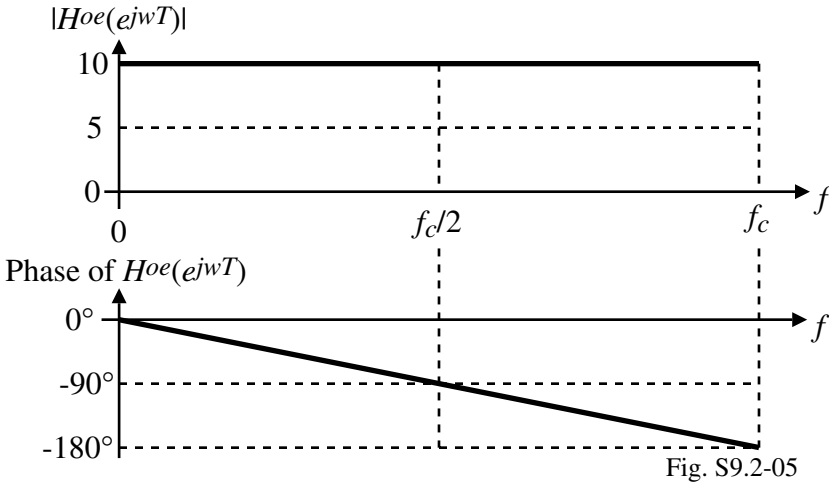


Fig. S9.2-05

Problem 9.2-06

Find $H^{oe}(z)$ ($=V^{e}_{out}(z)/V^{o}_{in}(z)$) of the switched capacitor circuit shown in Fig. P9.2-6. Replace z by $e^{j\omega T}$ and identify the magnitude and phase response of this circuit. Assume $C_1 = C_2$. Sketch the magnitude and phase response on a linear-linear plot from f=0 to f=f_c. What is the magnitude and phase at $f = 0.5f_c$?

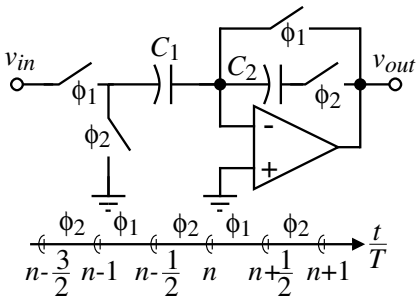
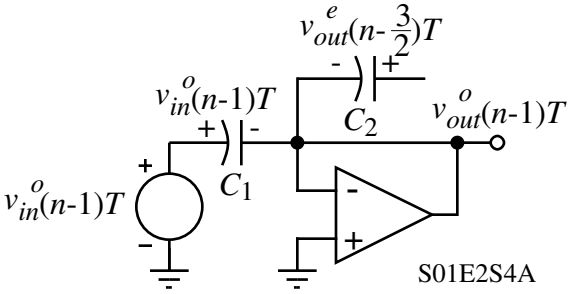


Figure P9.2-6

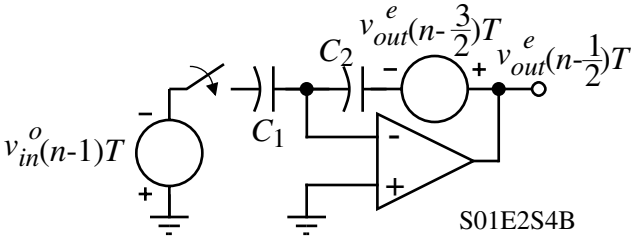
Solution

ϕ_1, t=(n-1)T: Circuit:



S01E2S4A

ϕ_2, t=(n-0.5)T: Circuit:



S01E2S4B

Writing the output,

$$v^{e}_{out}(n\text{-}0.5)) = v^{e}_{out}(n\text{-}1.5)) + \frac{C_1}{C_2} v^{o}_{in}(n\text{-}1)) \;\rightarrow V^{e}_{out}(z)) = z^{-1}\mathrm{V}^{e}_{out}(\mathrm{z}) + \frac{C_1}{C_2}\; z^{-0.5}V^{o}_{in}(z))$$

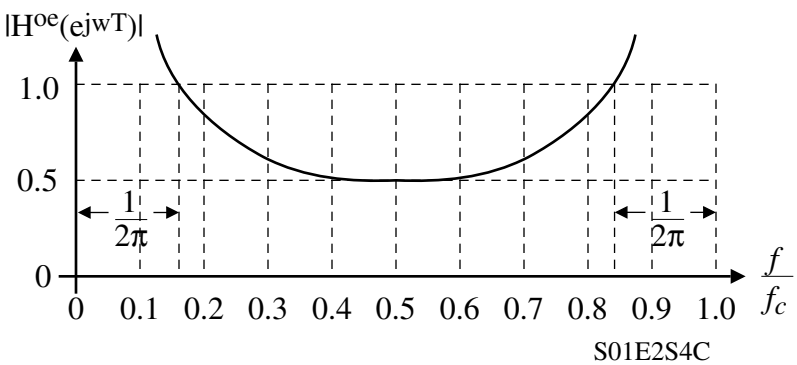
$$\therefore\; H^{oe}(z) = \frac{V^{e}_{out}(z)}{V^{o}_{in}(z)} = \frac{(C_1/C_2)z^{-0.5}}{1\text{-}z^{-1}}$$

Replacing z by $e^{j\omega T}$ gives $H^{oe}(e^{j\omega T}) = \dfrac{(C_1/C_2)e^{-j\omega T/2}}{1\text{-}e^{-j\omega T}} \mathrm{x} \dfrac{e^{j\omega T/2}}{e^{j\omega T/2}} = \dfrac{(C_1/C_2)}{e^{j\omega T/2}\text{-}e^{-j\omega T}}$

$$H^{oe}(e^{j\omega T}) = \frac{(C_1/C_2)}{2jsin(\omega T/2)} \mathrm{x} \frac{\omega T}{\omega T} = \frac{C_1}{j\omega C_2 f}\; \frac{\omega T/2}{sin(\omega T/2)} \quad \text{(note there is no phase error)}$$

If $C_1 = C_2$, then $H^{oe}(e^{j\omega T}) = \dfrac{f_c}{j2\pi f}\; \dfrac{\pi f/f_c}{sin(\pi f/f_c)}$

Sketch of frequency response:



f/f_c	$\lvert H^{oe}(e^{j2\pi f/f_c})\rvert$
$1/2\pi$	1
0.5	0.5
$1\text{-}0.5\pi$	1

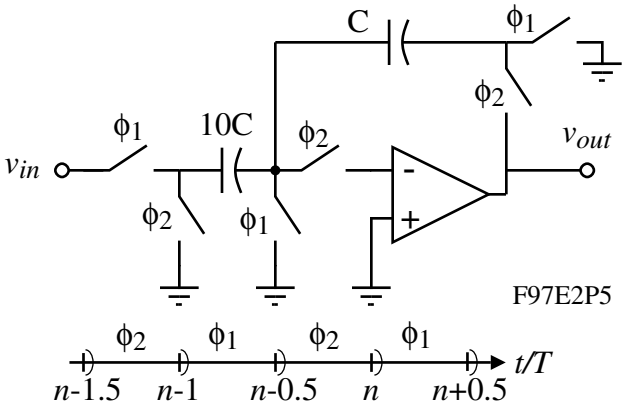
Phase shift is a constant -90°.

S01E2S4C

Problem 9.2-07

(a.) Find $H^{oo}(z)$ for the switched capacitor circuit shown. Ignore the fact that the op amp is open loop during the ϕ_1 phase and assume that the output is sampled during ϕ_2 and held during ϕ_1. Note that some switches are shared between the two switched capacitors.

(b.) Sketch the magnitude and phase of the sampled data frequency response from 0 to the clock frequency in Hertz.



Solution:

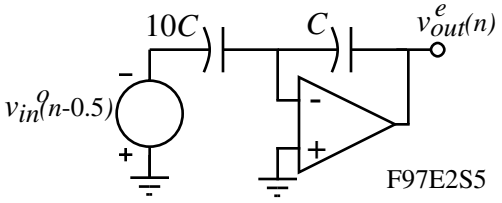
$\phi_1(n\text{-}0.5)$:

During this phase, the 10C capacitor is charged to $v_{in}^{o}(n\text{-}0.5)$ and the output is sampled and held.

$\phi_2(n)$:

Model for calculating $v_{out}^{e}(n)$,

$\therefore\ v_{out}^{e}(n) = 10v_{in}^{o}(n\text{-}0.5)$

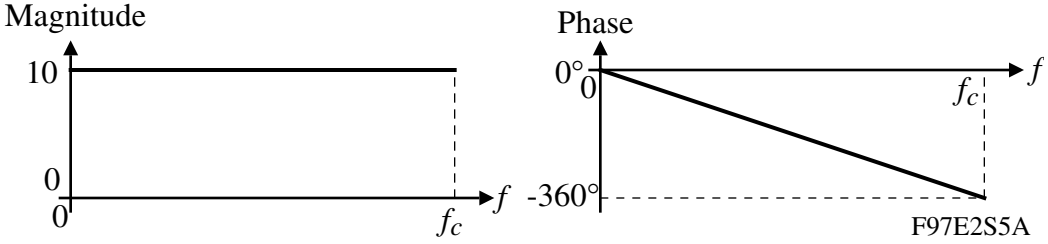


Since the output is sampled and held during the next phase period, we can write

$$v_{out}^{o}(n+0.5) = v_{out}^{e}(n) = 10v_{in}^{o}(n\text{-}0.5) \rightarrow V_{out}^{o}(z) = 10z^{-1}V_{in}^{o}(z)$$

or $\boxed{H^{oo}(z) = 10z^{-1}}$

b.)



Problem 9.2-08

In the circuit shown, the capacitor C_1 has been charged to a voltage of V_{in} ($v_{in}>0$). Assuming that C_2 is uncharged, find an expression for the output voltage, V_{out}, after the ϕ_1 clock is applied. Assume that rise and fall times of the ϕ_1 clock are slow enough so that the channel of the NMOS transistor switch tracks the gate voltage. The on and off voltages of ϕ_1 are 10V and 0V, respectively. Evaluate the dc offset at the output if the various parameters for this problem are V_T = 1V, $C_{gs} = C_{gd}$ = 100fF, C_1 = 5pF, and C_2 = 1pF.

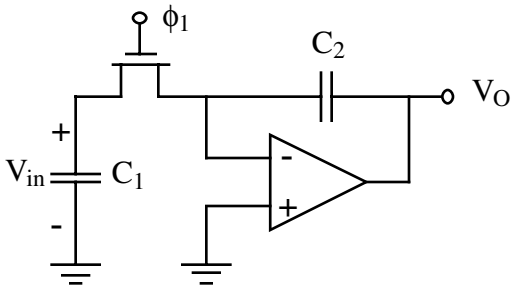


Figure P9.2-8

Solution

Since the problem does not give the value of V_{in} or the slope of the gate voltage, we shall assume that the contribution to the feedthrough due to the channel can be neglected. Therefore, the output voltage after the switch opens up can be expressed as,

$$V_o = -\frac{C_1}{C_2}V_{in} - \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_T) = -5V_{in} - \frac{1}{11} = -5V_{in} - \frac{1}{11}$$

The dc offset is 1/11V or 91mV.

A closer look at the problem reveals that there will also be feedthrough during the turn-on part of the ϕ_1 clock which should be considered. However, if we are going to consider this then we should also consider how C_1 was charged. It is most likely the complete circuit looks like the one shown.

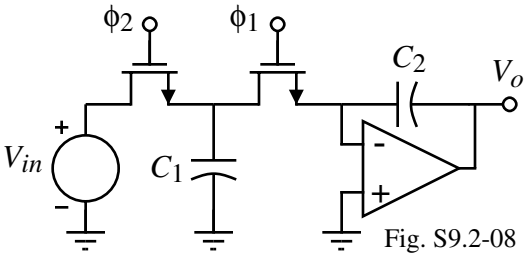


Fig. S9.2-08

When ϕ_2 is turned off, the voltage across C_1 is,

$$V_{C1}(\phi_2 \text{ off}) = V_{in} - \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_{in}+V_T) = V_{in} - \frac{1}{11}V_{in} - \frac{1}{11}$$

When $\phi_1$turns on, the voltage across C_1 is,

$$V_{C1}(\phi_1 \text{ on}) = V_{C1}(\phi_2 \text{ off}) + \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_T) = V_{in} - \frac{1}{11}V_{in} - \frac{1}{11} + \frac{1}{11} = V_{in} - \frac{1}{11}V_{in}$$

Finally, when $\phi_1$turns off, the voltage across C_1 is,

$$V_{C1}(\phi_1 \text{ off}) = -5V_{C1}(\phi_1 \text{ on}) - \left(\frac{C_{gd}}{C_{gd}+C_1}\right)(V_T) = 5V_{in} - \frac{5}{11}V_{in} - \frac{1}{11} = -\frac{51}{11}V_{in} - \frac{1}{11}$$

The dc offset is still the same as above.

Problem 9.2-09

A switched-capacitor amplifier is shown. What is the maximum clock frequency that would permit the ideal output voltage to be reached to within 1% if the op amp has a dc gain of 10,000 and a single dominant pole at -100 rads/sec.? Assume ideal switches.

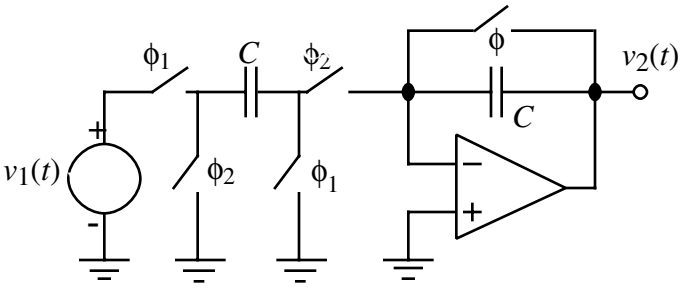
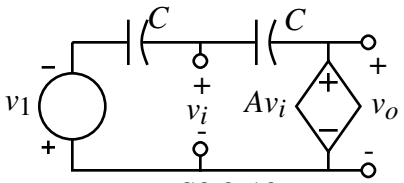


Figure P9.2-9

Solution

Model at $t=0^+$ for the ϕ_2 phase:



S9.2-12

$$\text{where } A = \frac{10^4}{\frac{s}{100}+1} \approx \frac{10^6}{s}$$

if $\omega >> 100$.

$$V_o(s) = AV_i(s) = A\left[+\frac{V_1(s)}{2} - \frac{V_o(s)}{2}\right] \quad \rightarrow \quad V_o(s)\left[1+\frac{A}{2}\right] = \frac{A}{2}V_1(a)$$

$$\therefore \quad V_o(s) = \frac{\frac{A}{2}}{1+\frac{A}{2}}V_1(a) = \frac{\frac{1}{2}}{\frac{1}{A}+\frac{1}{2}}V_1(a) \approx \frac{\frac{1}{2}}{\frac{s}{10^6}+\frac{1}{2}}V_1(a) = \frac{0.5\text{x}10^6}{s+0.5\text{x}10^6}V_1(a)$$

$$v_o(t) = \mathrm{L}^{-1}\left[\frac{0.5\text{x}10^6}{s+0.5\text{x}10^6}\cdot\frac{V_1}{s}\right] = \frac{A}{s} + \frac{B}{s+0.5\text{x}10^6}$$

$$A = \frac{0.5\text{x}10^6}{s+0.5\text{x}10^6}V_1\Big|_{s=0} = V_1 \quad \text{and} \quad B = \frac{0.5\text{x}10^6}{s}V_1\Big|_{s=0.5\text{x}10^6} = -V_1$$

$$\therefore \quad v_o(t) = V_1[1-e^{-0.5\text{x}10^6 t}]$$

Let $t = T$ correspond to $v_o(T) = 0.99V_1$

$$\therefore \quad 0.99V_1 = V_1[1-e^{-0.5\text{x}10^6 T}] \quad \rightarrow \quad 100 = e^{0.5\text{x}10^6 T}$$

$$ln(100) = 0.5\text{x}10^6 T \quad \rightarrow \quad T = 2\text{x}10^{-6} ln(100) = 9.21\mu\text{s}$$

Assuming a square wave, T would be half the period so the minimum clock frequency would be

$$f_{clock}(\text{min}) = \frac{2}{T} = \underline{\underline{54.287\text{kHz}}}$$

Problem 9.2-10

The switched capacitor circuit in Fig. 9.2-9 is an amplifier that avoids shorting the output of the op amp to ground during the ϕ_1 phase period. Use the clock scheme shown along with the timing and find the z-domain transfer function, $H^{oo}(z)$. Sketch the magnitude and phase shift of this amplifier from zero frequency to the clock frequency, f_c.

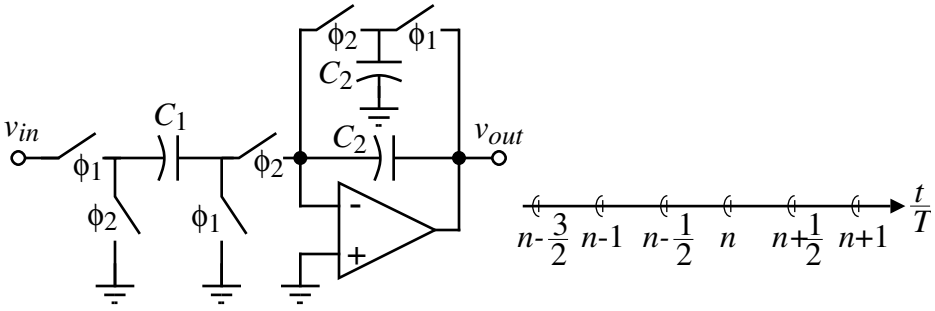
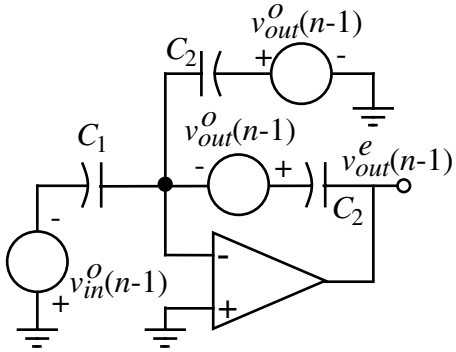


Fig. P9.2-13

Solution

ϕ_1: $(n\text{-}1) \le t/T < (n\text{-}0.5)$

$v_{c1}^{o}(n\text{-}1) = v_{in}^{o}(n\text{-}1)$ and $v_{c2}^{o}(n\text{-}1) = v_{out}^{o}(n\text{-}1)$



ϕ_2: $(n\text{-}0.5) \le t/T < (n)$

$$v_{out}^{e}(n\text{-}0.5) = v_{out}^{o}(n\text{-}1) + \frac{C_1}{C_2} v_{in}^{o}(n\text{-}1) - \frac{C_2}{C_2} v_{out}^{o}(n\text{-}1)$$

or

$$v_{out}^{e}(n\text{-}0.5) = \frac{C_1}{C_2} v_{in}^{o}(n\text{-}1)$$

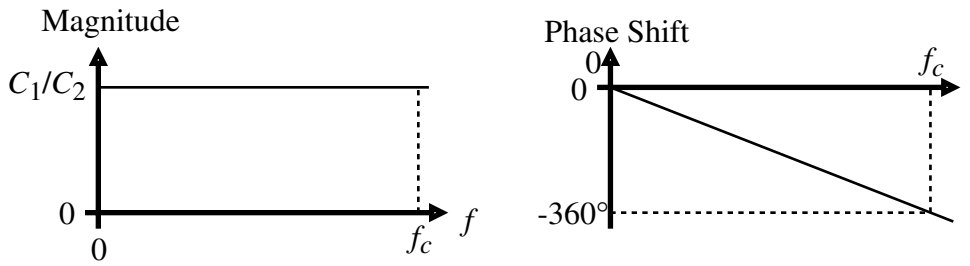
ϕ_1: $(n) \le t/T < (n\text{+}0.5)$

$$v_{out}^{o}(n) = v_{out}^{e}(n\text{-}1) = \frac{C_1}{C_2} v_{in}^{o}(n\text{-}1) \quad \rightarrow \quad V_{out}^{o}(z) = z^{-1} \frac{C_1}{C_2} V_{in}^{o}(z) \quad \rightarrow \quad \boxed{H^{oo}(z) = \frac{C_1}{C_2} z^{-1}}$$

Substitituting z^{-1} by $e^{-j\omega T}$ gives

$$H^{oo}(e^{j\omega T}) = \frac{C_1}{C_2} e^{-j\omega T}$$

The magnitude and phase response is given below.



Problem 9.2-11

(a.) Give a schematic drawing of a switched capacitor realization of a voltage amplifier having a gain of H^{oo} = +10V/V using a two-phase nonoverlapping clock. Assume that the input is sampled on the ϕ_1 and held during ϕ_2. Use op amps, capacitors, and switches with ϕ_1 or ϕ_2 indicating the phase the switch is closed.

(b.) Give a schematic of the circuit in (a.) that reduces the number of switches to a minimum number with the circuit working correctly. Assume the op amp is ideal.

(c.) Convert the circuit of (a.) to a differential implementation using the differential-in, differential-out op amp shown in Fig. P9.2-11.

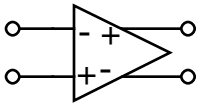
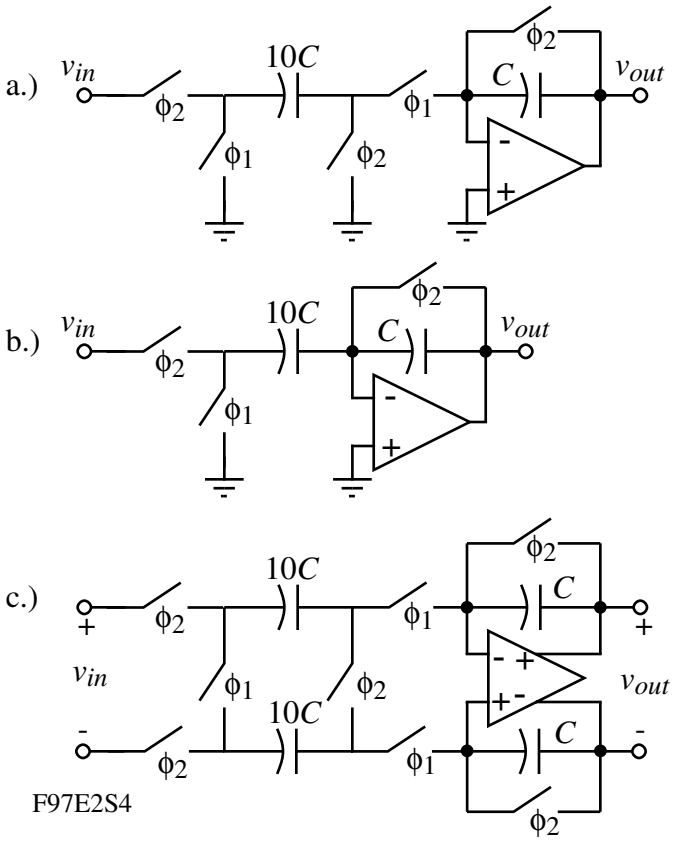


Figure P9.2-11

Solution

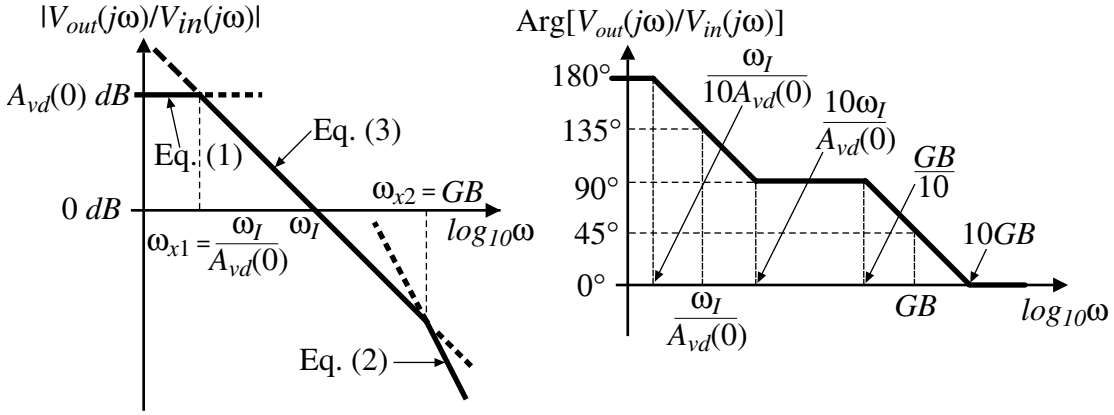


Problem 9.3-01

Over what frequency range will the integrator of Ex. 9.3-1 have a ±1° phase error?

Solution

Assuming the integrator frequency response can be represented as shown below.



The integrator phase error on the low side of the useful band is given as,

$$\text{Error} = 90° - \tan^{-1}\left(\frac{\omega_L}{\omega_I/A_{vd}(0)}\right) = 1° \quad \rightarrow \quad \omega_L = 57.29\,\frac{\omega_I}{A_{vd}(0)}$$

The integrator phase error on the high side of the useful band is given as,

$$\text{Error} = \tan^{-1}\left(\frac{\omega_H}{GB}\right) = 1° \quad \rightarrow \quad \omega_H = \frac{GB}{57.29}$$

If $A_{vd}(0)$, ω_I, and GB are given, the useful range is from ω_L to ω_H.

Problem 9.3-02

Show how Eq. (9.3-12) is developed from Fig. 9.3-4(b.).

Solution

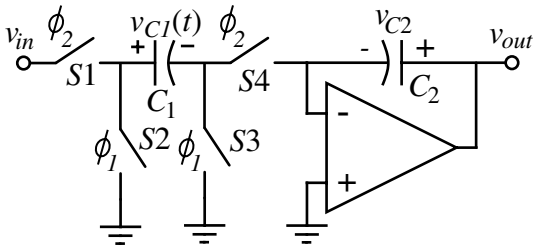


Fig. 9.3-4(b.)

Problem 9.3-03

Find the $H^{eo}(j\omega T)$ transfer function for the inverting integrator of Fig. 9.3-4b and compare with the $H^{ee}(j\omega T)$ transfer function.

Solution

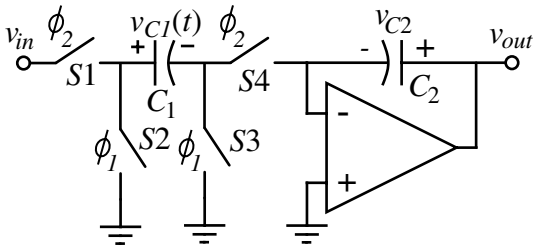


Fig. 9.3-4(b.)

Problem 9.3-04

An inverting, switched-capacitor integrator is shown. If the gain of the op amp is A_o, find the z-domain transfer function of this integrator. Identify the ideal part of the transfer function and the part due to the finite op amp gain, A_o. Find an expression for the excess phase due to A_o.

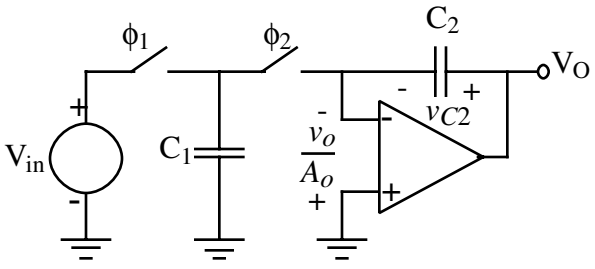


Figure P9.3-4

Solution

Let us use charge conservation to solve the problem.

$$C_2 v_{C2}(nT) = C_2 v_{C2}[(n\text{-}1)T] - C_1[v_{in}\,(n\text{-}1)T + v_o(nT)/A_o]$$

or

$$V_{C2}(z) = z^{-1}V_{C2}(z) - \frac{C_1}{C_2}z^{-1}V_{in}(z) - \frac{C_1}{C_2}\frac{V_o(z)}{A_o}$$

$$V_{C2}(z)[1\text{-}\,z^{-1}] = -\alpha\, z^{-1}V_{in}(z) - \alpha\frac{V_o(z)}{A_o}, \qquad \text{where } \alpha = \frac{C_1}{C_2}$$

$$V_{C2}(z) = \frac{-\alpha\, z^{-1}}{1\text{-}\,z^{-1}}V_{in}(z) - \frac{-\alpha/A_o}{1\text{-}\,z^{-1}}V_o(z)$$

$$\therefore \quad V_o(z) = V_{C2}(z) - \frac{V_o(z)}{A_o} = \frac{-\alpha\, z^{-1}}{1\text{-}\,z^{-1}}V_{in}(z) - \frac{-\alpha/A_o}{1\text{-}\,z^{-1}}V_o(z) - \frac{V_o(z)}{A_o}\,\text{x}\,\frac{1\text{-}\,z^{-1}}{1\text{-}\,z^{-1}}$$

$$V_o(z)\left[1\text{-}\,z^{-1} + \frac{\alpha}{A_o} + \frac{1\text{-}\,z^{-1}}{A_o}\right] = -\alpha\, z^{-1}V_{in}(z)$$

$$\therefore \quad H(z) = \frac{V_o(z)}{V_{in}(z)} = \frac{-\alpha\, z^{-1}}{1\text{-}\,z^{-1} + \dfrac{1+\alpha\,\text{-}\,z^{-1}}{A_o}} = \left(\frac{-\alpha\, z^{-1}}{1\text{-}\,z^{-1}}\right)\left(\frac{1}{1+\dfrac{1+\alpha\,\text{-}\,z^{-1}}{A_o(1\text{-}\,z^{-1})}}\right)$$

The first bracket is the ideal term and the second bracket is the term due to A_o.

To evaluate the excess phase due to A_o we replace z by $e^{j\omega T}$.

$$H(e^{j\omega T}) = \frac{1}{1+\dfrac{1+\alpha\,\text{-}\,z^{-1}}{A_o(1\text{-}\,z^{-1})}} = \frac{1}{1+\dfrac{(1+\alpha)\,e^{j\omega T/2}}{A_o(e^{j\omega T/2}\text{-}\,e^{-j\omega T/2})} + \dfrac{e^{j\omega T/2}}{A_o(e^{j\omega T/2}\text{-}\,e^{-j\omega T/2})}}$$

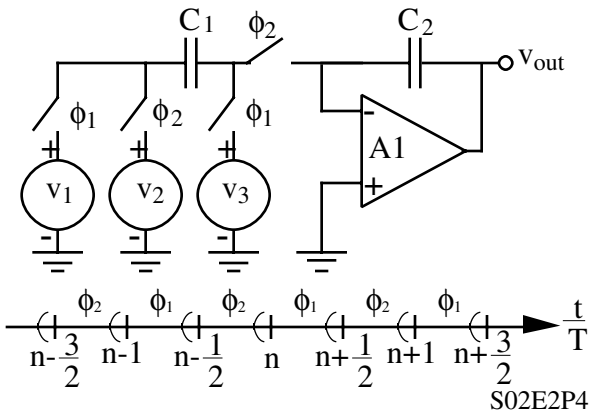
$$= \frac{1}{1\;\text{-}\;\text{j}\left(\dfrac{1+\alpha}{2A_o}\right)\left(\dfrac{cos(\omega T/2) + \text{j}sin(\omega T/2)}{sin(\omega T/2)}\right) + \dfrac{j}{2A_o}\left(\dfrac{cos(\omega T/2) + \text{j}sin(\omega T/2)}{sin(\omega T/2)}\right)}$$

$$= \frac{1}{1 + \dfrac{2+\alpha}{A_o} - \text{j}\,\dfrac{\alpha}{2A_o}cot(\omega T/2)} \rightarrow \text{Arg}[H(e^{j\omega T})] = -\tan^{-1}\left[\frac{\dfrac{\alpha}{2A_o}cot(\omega T/2)}{1 + \dfrac{2+\alpha}{A_o}}\right]$$

$$\therefore \text{ Excess phase} = -\tan^{-1}\left[\frac{\alpha\, cot(\omega T/2)}{2A_o + 4 + 2\alpha}\right] \approx -\tan^{-1}\left[\frac{\alpha}{2A_o\, tan(\omega T/2)}\right] \approx -\frac{\alpha}{2A_o\, tan(\omega T/2)}$$

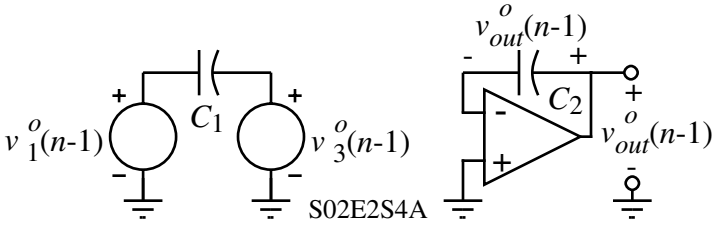
Problem 9.3-05

For the switched-capacitor circuit shown find $V_{OUT}^{o}(z)$ as a function of $V_1^o(z)$, $V_2^o(z)$, and $V_3^o(z)$ assuming the clock is a two-phase, nonoverlapping clock. Assume that the clock frequency is much greater than the signal bandwidth and find an approximate expression for $V_{out}(s)$ in terms of $V_1(s)$, $V_2(s)$, and $V_3(s)$. Assume that the inputs are sampled and held where necessary.

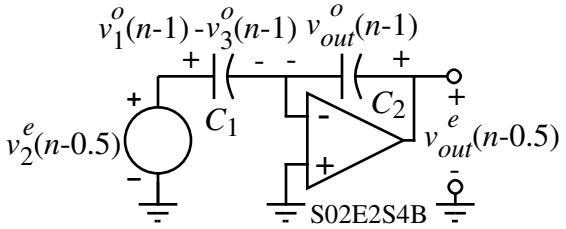


Solution

ϕ_1, $t = (n\text{-}1)T$: Model:



ϕ_2, $t = (n\text{-}0.5)T$: Model:



$$v_{out}^{e}(n\text{-}0.5) = v_{out}^{o}(n\text{-}1) - \frac{C_1}{C_2}v_2^e(n\text{-}0.5) - \frac{C_1}{C_2}v_1^o(n\text{-}1) + \frac{C_1}{C_2}v_3^o(n\text{-}1)$$

ϕ_1, $t = (n)T$:

$$v_{out}^{o}(n) = v_{out}^{o}(n\text{-}1) - \frac{C_1}{C_2}v_2^e(n\text{-}0.5) + \frac{C_1}{C_2}v_1^o(n\text{-}1) - \frac{C_1}{C_2}v_3^o(n\text{-}1)$$

$$\therefore \quad V_{out}^{o}(z) = z^{-1}V_{out}^{o}(n\text{-}1) - z^{-0.5}\frac{C_1}{C_2}V_2^e(z) + z^{-1}\frac{C_1}{C_2}V_1^o(z) - z^{-1}\frac{C_1}{C_2}V_3^o(z)$$

Replacing $V_2^e(z)$ by $z^{-0.5}V_2^o(z)$ gives

$$V_{out}^{o}(z) = z^{-1}V_{out}^{o}(n\text{-}1) - z^{-1}\frac{C_1}{C_2}V_2^o(z) + z^{-1}\frac{C_1}{C_2}V_1^o(z) - z^{-1}\frac{C_1}{C_2}V_3^o(z)$$

$$V_{out}^{o}(z) = -\frac{z^{-1}}{1\text{-}z^{-1}}[-V_1^o(z) + V_2^o(z) + V_3^o(z)]$$

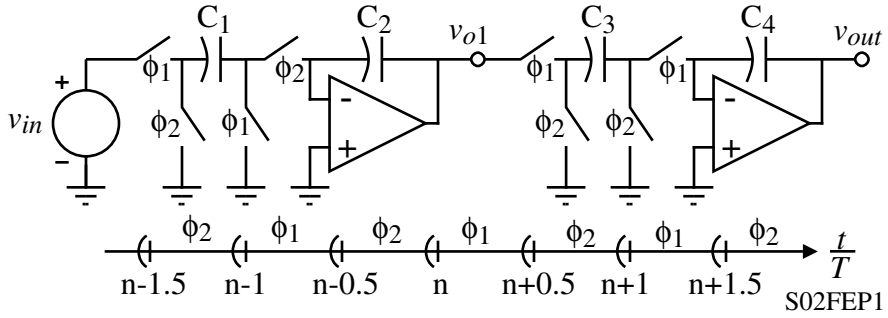
Replacing $1\text{-}z^{-1}$ by sT and z^{-1} by 1 gives,

$$V_{out}^{o}(s) = -\frac{1}{sT}[-V_1^o(s) + V_2^o(s) + V_3^o(s)]$$

$$\therefore \quad \boxed{V_{out}^{o}(s) = \frac{1}{sT}[V_1^o(s) - V_2^o(s) - V_3^o(s)]}$$

Problem 9.3-06

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oo}(z)$. (2.) Replace z by $e^{j\omega T}$ and plot the magnitude and phase of this switched capacitor circuit from 0 Hz to the clock frequency, f_c, if $C_1 = C_3$ and $C_2 = C_4$. Assume that the op amps are ideal for this problem. (3.) What is the multiplicative magnitude error and additive phase error at $f_c/2$?



Solution

(1.) ϕ_1 (n-1≤t/T<n-0.5):

$$q_{C1}^{o}(n\text{-}1) = C_1 v_{in}^{o}(n\text{-}1) \qquad \text{and} \qquad q_{C2}^{o}(n\text{-}1) = C_2 v_{o1}^{o}(n\text{-}1)$$

ϕ_2 (n-0.5≤t/T<n):

$$q_{C2}^{e}(n\text{-}0.5) = q_{C2}^{o}(n\text{-}1) + q_{C1}^{o}(n\text{-}1) \qquad \text{and} \qquad q_{C4}^{e}(n\text{-}0.5) = C_4 v_{out}^{e}(n\text{-}0.5)$$

ϕ_1 (n≤t/T<n+0.5):

$$q_{C2}^{o}(n) = q_{C2}^{e}(n\text{-}0.5) = q_{C2}^{o}(n\text{-}1) + q_{C1}^{o}(n\text{-}1)$$

$$v_{o1}^{o}(n) = v_{o1}^{o}(n\text{-}1) + \frac{C_1}{C_2} v_{in}^{o}(n\text{-}1) \qquad \rightarrow \qquad V_{o1}^{o}(z) = z^{-1} V_{o1}^{o}(z) + \frac{C_1}{C_2} V_{in}^{o}(z)$$

$$\therefore \qquad V_{o1}^{o}(z) = \frac{C_1/C_2}{z\text{-}1} V_{in}^{o}(z)$$

Also, $q_{C3}^{o}(n) = C_3\, v_{o1}^{o}(n)$ and $q_{C4}^{o}(n) = q_{C4}^{e}(n\text{-}0.5) - q_{C3}^{o}(n)$

$$q_{C4}^{o}(n) = q_{C4}^{o}(n\text{-}1) - q_{C3}^{o}(n) \qquad \rightarrow \qquad V_{out}^{o}(z) = z^{-1} V_{o1}^{o}(z) - \frac{C_3}{C_4} V_{o1}^{o}(z)$$

$$\therefore \qquad V_{out}^{o}(z) = \frac{-(C_3/C_4)z^{-1}}{z\text{-}1} V_{in}^{o}(z)$$

$$\therefore \qquad V_{out}^{o}(z) = \left(\frac{-(C_3/C_4)z^{-1}}{z\text{-}1}\right)\left(\frac{C_1/C_2}{z\text{-}1}\right) V_{in}^{o}(z) \quad \rightarrow \quad H_{oo}(z) = \frac{V_{out}^{o}}{V_{in}^{o}} = -\left(\frac{C_1 C_3}{C_2 C_4}\right)\frac{z}{(z\text{-}1)^2}$$

Problem 9.3-06 – Continued

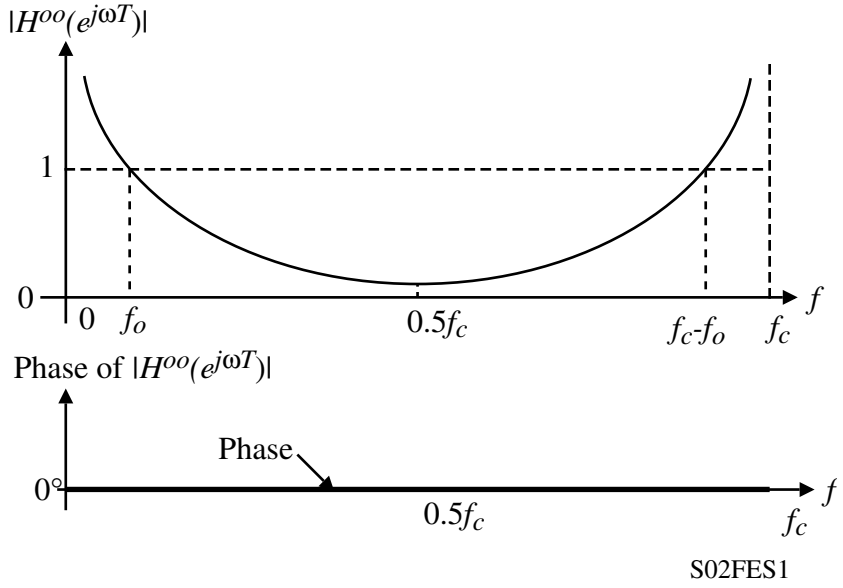
$$\therefore \quad H^{oo}(e^{j\omega T}) = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{e^{j\omega T}}{(e^{j\omega T}-1)^2} = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{1}{(e^{j\omega T/2}-e^{-j\omega T/2})^2} = -\left(\frac{C_1C_3}{C_2C_4}\right)\frac{1}{(2j\sin(\omega T/2))^2}$$

$$= -\left(\frac{C_1C_3}{C_2C_4}\right)\left(\frac{(\omega T/2)}{j\omega T\sin(\omega T/2)}\right)^2 = \left(\frac{-C_1}{j\omega TC_2}\frac{\omega T/2}{\sin(\omega T/2)}\right)\left(\frac{C_3}{j\omega TC_4}\frac{\omega T/2}{\sin(\omega T/2)}\right)$$

$$= \left(\frac{-\omega_{o1}}{j\omega}\right)\left(\frac{-\omega_{o2}}{j\omega}\right)\left(\frac{(\omega T/2)}{\sin(\omega T/2)}\right)^2 = \left(\frac{-\omega_o}{j\omega}\right)^2\left(\frac{(\omega T/2)}{\sin(\omega T/2)}\right)^2$$

If $C_1 = C_3$ and $C_2 = C_4$, $\omega_{o1} = C_1/(TC_2)$, and $\omega_{o2} = C_3/(TC_4)$.

The frequency response is plotted below.



S02FES1

$$\therefore \quad \text{The magnitude error} = \left(\frac{(\omega T/2)}{\sin(\omega T/2)}\right)^2 = \left(\frac{(\pi/2)}{\sin(\pi/2)}\right)^2 = \frac{\pi^2}{4} = 2.467$$

Phase error = 0°

Problem 9.3-07

Find $H^{oo}(z)$ ($=V^{o}_{out}(z)/V^{o}_{in}(z)$) of the switched capacitor circuit shown. Replace z by $e^{j\omega t}$ and identify the magnitude and phase response of this circuit. Assume $C_1/C_2 = \pi/25$. Sketch the exact magnitude and phase response on a linear-linear plot from f=0 to f=f_c. What is the magnitude and phase at f = $0.5f_c$? Assume that the op amp is ideal.

Solutions

ϕ_2; $(n\text{-}0.5)<t/T<n$

At $t = 0^+$ we have the following model:

We can write,

$$v^{e}_{out}(n\text{-}0.5) = v^{o}_{out}(n\text{-}1) - \frac{C_1}{C_2} v^{o}_{in}(n\text{-}1)$$

But $$v^{e}_{out}(n) = v^{e}_{out}(n\text{-}0.5) = v^{o}_{out}(n\text{-}1) - \frac{C_1}{C_2} v^{o}_{in}(n\text{-}1)$$

$$\therefore \qquad V^{o}_{out}(z) = z^{-1}V^{o}_{out}(z) - \frac{C_1}{C_2} z^{-1}V^{o}_{in}(z) \qquad \rightarrow \qquad H^{oo}(z) = \frac{\frac{C_1}{C_2}z^{-1}}{1\text{-}z^{-1}}$$

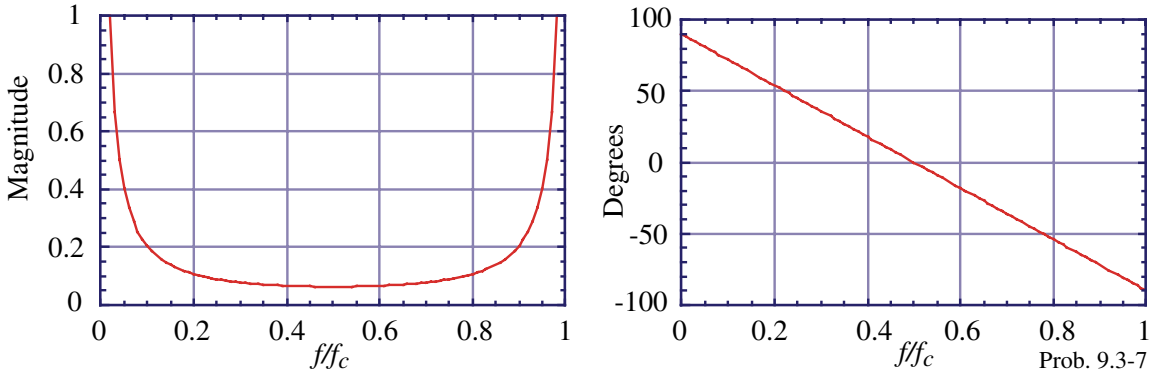
$$H^{oo}(e^{j\omega T}) = -\frac{C_1}{C_2}\left(\frac{e^{-j\omega T}}{1\text{-}e^{-j\omega T}}\right)\frac{e^{j\omega T/2}}{e^{j\omega T/2}} = -\frac{C_1}{C_2}\frac{e^{-j\omega T/2}}{e^{j\omega T/2}\text{-}\ e^{-j\omega T/2}} = -\frac{C_1}{C_2}\frac{e^{-j\omega T/2}}{2j\,\sin(\omega T/2)} \text{ x } \frac{\omega T}{\omega T}$$

$$= \left(-\frac{C_1}{jC_2\omega T}\right)\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)(e^{-j\omega T/2}) = \left(-\frac{\omega_o}{j\omega}\right)\left(\frac{\omega T/2}{\sin(\omega T/2)}\right)(e^{-j\omega T/2})$$

For $f = 0.5f_c$ we get $\frac{\omega T}{2} = \frac{2\pi f_c}{2\cdot 2f_c} = \frac{\pi}{2}$ and $\omega_o = \frac{C_1}{C_2 T} = \frac{\pi}{25}f_c$

$$\therefore \quad |H^{oo}(e^{j\pi})| = \left(\frac{f_c/50}{f_c/2}\right)\left(\frac{\pi/2}{\sin(\pi/2)}\right) = \frac{1}{25}\frac{\pi}{2} = \underline{\underline{0.06283}} \text{ and } \text{Arg}[H^{oo}(e^{j\pi})] = +90°\text{-}90° = \underline{\underline{0°}}$$

Plots:



Prob. 9.3-7

Problem 9.3-08

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{ee}(z)$. (2.) If $C_2 = 0.2\pi C_1$, plot the magnitude and phase response of the switched capacitor circuit from 0 rps to the clock frequency (ω_c). Assume that the op amp is ideal for this problem. It may be useful to remember that Eulers formula is $e^{\pm jx} = \cos(x) \pm j\sin(x)$.

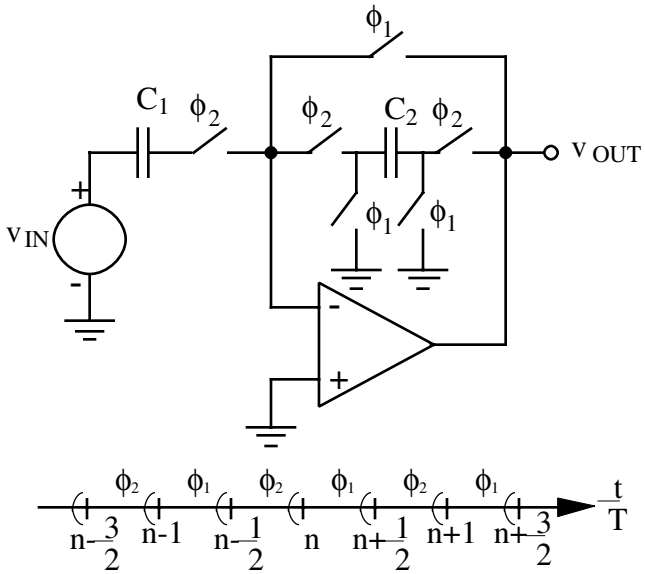


Figure P9.3-8

Solution

ϕ_1: $t = (n\text{-}1)T$

The capacitor, C_1, simply holds the voltage, $v_{in}^e(n\text{-}1.5)$ and $C_2 = 0$V.

ϕ_2: $t = (n\text{-}0.5)T$

The model for this phase is given.

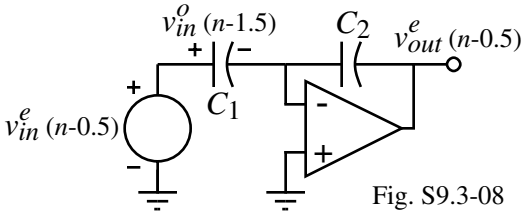


Fig. S9.3-08

The equation for this phase can be written as,

$$v_{out}^e(n\text{-}0.5) = -\frac{C_1}{C_2}\, v_{in}^e(n\text{-}0.5) + \frac{C_1}{C_2}\, v_{in}^e(n\text{-}1.5)$$

Converting to the z-domain gives,

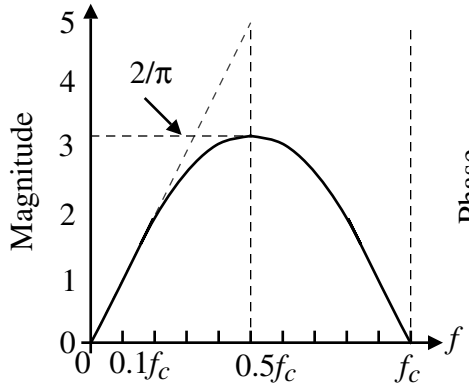
$$z^{-1/2}V_{out}^e(z) = -\frac{C_1}{C_2} z^{-1/2}V_{in}^e(z) + \frac{C_1}{C_2} z^{-3/2}V_{in}^e(z) \quad \rightarrow \quad V_{out}^e(z) = -\frac{C_1}{C_2} V_{in}^e(z) + \frac{C_1}{C_2} z^{-1}V_{in}^e(z)$$

$$\therefore \qquad \frac{V_{out}^e(z)}{V_{in}^e(z)} = -\frac{C_1}{C_2}(1\text{-}z^{-1}) \qquad \rightarrow \qquad \frac{V_{out}^e(j\omega)}{V_{in}^e(j\omega)} = H^{ee}(j\omega) = -\frac{C_1}{C_2}(1\text{-}e^{-j\omega T}) x \frac{e^{j\omega T/2}}{e^{j\omega T/2}}$$

$$H^{ee}(j\omega) = \frac{5}{\pi}\left(\frac{e^{j\omega T/2} - e^{-j\omega T/2}}{e^{j\omega T/2}}\right) = \frac{5}{\pi}[j2\sin(\omega T/2)]\, e^{-j\omega T/2} = \frac{10}{\pi}\frac{j\omega T}{2}\left(\frac{\sin(\omega T/2)}{\omega T/2}\right)e^{-j\omega T/2}$$

$$H^{ee}(j\omega) = j\frac{10f}{f_c}\left(\frac{\sin(\omega T/2)}{\omega T/2}\right)e^{-j\omega T/2}$$

Plotting gives,



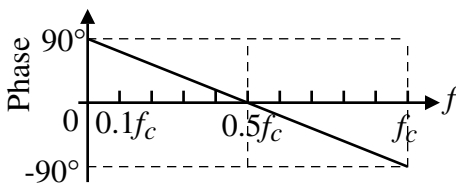
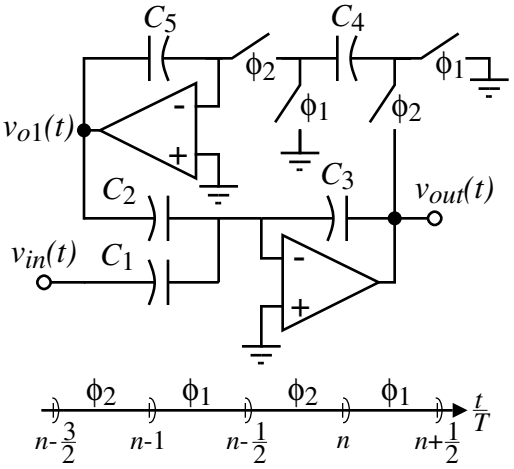


Fig. S9.3-08A

Problem 9.3-09

Find the z-domain transfer function, $H^{oo}(z)$, for the circuit shown. Assume that $C_2 = C_3 = C_4 = C_5$. Also, assume that the input is sampled during ϕ_1 and held through ϕ_2. Next, let the clock frequency be much greater than the signal frequency and find an expression for $H^{oo}(j\omega)$. What kind of circuit is this?



F97FEP2

Solution

ϕ_1: $n\text{-}1<(t/T)\le n\text{-}0.5$

$$v_{C4}^{o}(n\text{-}0.5) = v_{out}^{o}(n\text{-}0.5)$$

$$v_{out}^{o}(n\text{-}0.5) = -\frac{C_1}{C_3} v_{in}^{o}(n\text{-}0.5) - \frac{C_2}{C_3} v_{o1}(n\text{-}0.5) = v_{out}^{e}(n\text{-}1)$$

ϕ_2: $n\text{-}0.5<(t/T)\le n$

$$v_{o1}^{e}(n) = v_{o1}^{o}(n\text{-}0.5) - \frac{C_4}{C_5} v_{out}^{e}(n) \quad \text{and} \quad v_{out}^{e}(n) = -\frac{C_2}{C_3} v_{o1}^{e}(n) - \frac{C_1}{C_3} v_{in}^{e}(n)$$

$$\therefore \; v_{out}^{e}(n) = -\frac{C_2}{C_3}\left[v_{o1}^{o}(n\text{-}0.5) - \frac{C_4}{C_5} v_{out}^{e}(n) \right] - \frac{C_1}{C_3} v_{in}^{e}(n)$$

ϕ_1: $n<(t/T)\le n+0.5$

$$v_{out}^{o}(n+0.5) = -\frac{C_1}{C_3} v_{in}^{o}(n+0.5) - \frac{C_2}{C_3} v_{o1}^{o}(n+0.5) \rightarrow V_{out}^{o}(z) = -\frac{C_1}{C_3} V_{in}^{o}(z) - \frac{C_2}{C_3} V_{o1}^{o}(z)$$

but, $$v_{o1}^{o}(n+0.5) = v_{o1}^{e}(n) = v_{o1}^{o}(n\text{-}0.5) + \frac{C_4}{C_5} v_{out}^{o}(n\text{-}0.5)$$

$$V_{o1}^{o}(z) = z^{-1} V_{o1}^{o}(z) - \frac{C_4}{C_5} V_{out}^{o}(z) \rightarrow \qquad V_{o1}^{o}(z)[1\text{-}z^{-1}] = -\frac{C_4}{C_5} V_{out}^{o}(z)$$

Substituting into the above expression for $V_{out}^{o}(z)$ gives

$$V_{out}^{o}(z) = -\frac{C_1}{C_3} V_{in}^{o}(z) + \frac{C_2}{C_3}\left(\frac{C_4}{C_5}\frac{1}{1\text{-}z^{-1}}\right) V_{out}^{o}(z) \quad \rightarrow \quad H^{oo}(z) = \frac{-C_1/C_3}{1 - \left(\frac{C_2 C_4}{C_3 C_5}\right)\frac{1}{1\text{-}z^{-1}}}$$

If $C_2C_4 = C_3C_5$, then $\boxed{H^{oo}(z) = \frac{C_1}{C_3}\left[\frac{1\text{-}z^{-1}}{z^{-1}}\right]} \rightarrow H^{oo}(s) \approx \frac{C_1}{C_3}\left[\frac{1\text{-}(1\text{-}sT)}{1}\right] = \frac{C_1}{C_3} sT$

(This is a lot easier with z-domain models.)

$$\therefore \quad \boxed{H^{oo}(j\omega) \approx \frac{j\omega}{C_3/C_1 T} = \frac{j\omega}{\omega_D} \text{ where } \omega_D = \frac{C_3}{TC_1}}$$

This circuit is a noninverting switched capacitor differentiator.

Problem 9.4-01

Repeat Ex. 9.4-1 for the positive switched capacitor transresistance circuit of Fig. 9.4-3.

Solution

TBD

Problem 9.4-02

Use the z-domain models to verify Eqs. (9.2-19) and (9.2-23) of Sec. 9.2 for Fig. 9.2-4(b.).

Solution

TBD

Problem 9.4-03

Repeat Ex. 9.4-5 assuming that the op amp is ideal (gain = ∞). Compare with the results of Ex. 9.4-5 (Hint: use Fig. 9.4-8b).

Solution

TBD

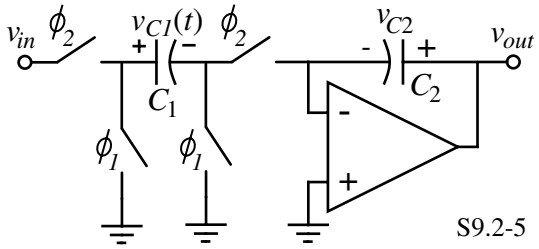
Problem 9.4-04

Repeat Ex. 9.4-5 assuming the op amp gain is 100V/V. Compare with the results of Ex. 9.4-5.

Solution

Problem 9.4-05

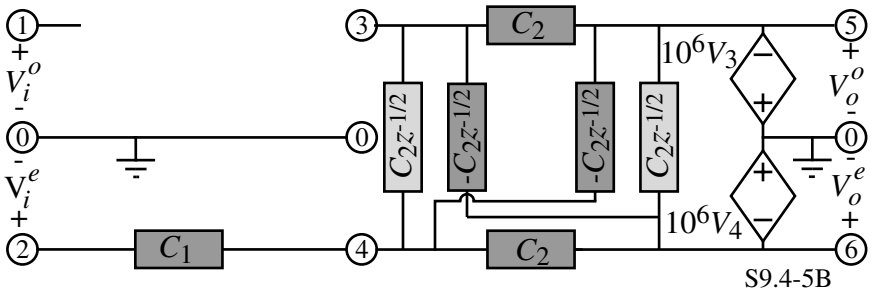
Repeat Ex. 9.4-5 for the inverting switched capacitor integrator in Fig. 9.3-4(b).



S9.2-5

Solution

The z-domain model for this circuit is shown below.



S9.4-5B

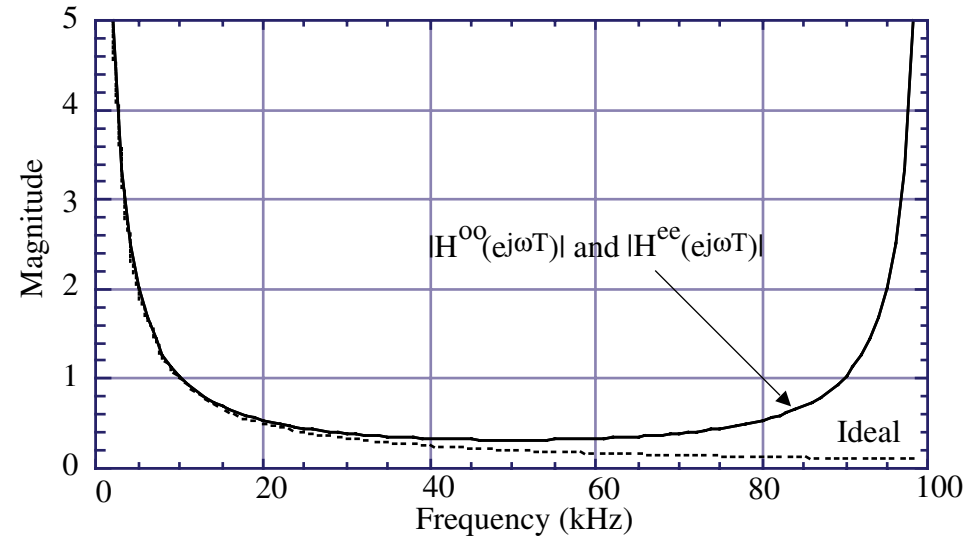
$$\omega_I = \frac{1}{R_1 C_2} = \frac{f_c C_1}{C_2} \quad \Rightarrow \quad \frac{C_1}{C_2} = \frac{2\pi f_I}{f_c} = \frac{2\pi(10\text{kHz})}{100\text{kHz}} = \frac{\pi}{5} = 0.62832$$

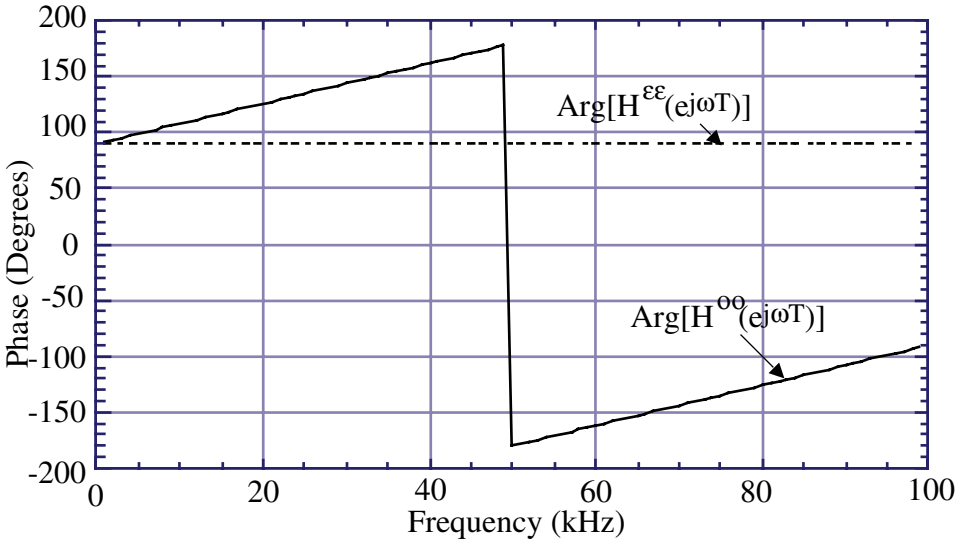
$\therefore$ Let C_2 = 1F and C_1 = 0.62832F

```
SPICE Input File
Problem 9.4-5 Solution
R24 2 5 1.592
X43PC2 4 3 43 DELAY
G43 4 3 43 0 1
R35 3 5 1.0
X56PC2 5 6 56 DELAY
G56 5 6 56 0 1
R46 4 6 1.0
X36NC2 3 6 36 DELAY
G36 6 3 36 0 1
X45NC2 4 5 45 DELAY
G45 5 4 45 0 1
EODD 6 0 4 0 1E6
EVEN 5 0 3 0 1E6
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5U
RDO 3 0 1K
.ENDS DELAY
.AC LIN 99 1K 99K
.PRINT AC V(6) VP(6) V(5) VP(5)
.PROBE
.END
```

Problem 9.4-05 - Continued

Plot of the results is below.





Solution 9.4-5

Problem 9.5-01

Develop Eq. (9.5-6) for the inverting low pass circuit obtained from Fig. 9.1-5(a.) by reversing the phases of the leftmost two switches. Verify Eq. (9.5-7).

Solution

TBD

Problem 9.5-02

Use SPICE to simulate the results of Ex. 9.5-1.

Solution

The SPICE model for this problem is given as

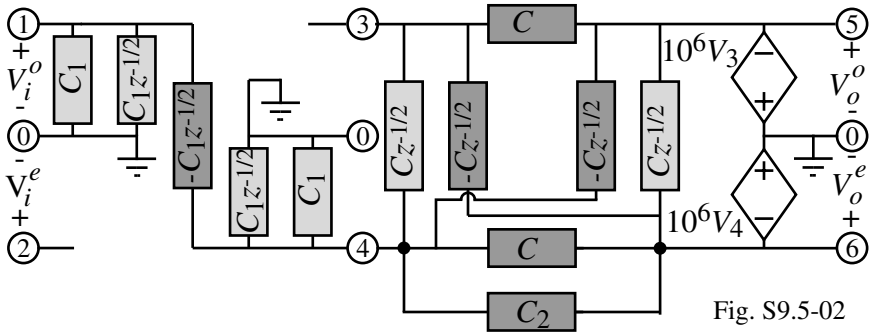


Fig. S9.5-02

The SPICE input file is:

```
PROBLEM 9.5-2 SOLUTION
VIN 1 0 DC 0 AC 1
R10C1 1 0 1.592
X10PC1 1 0 10 DELAY
G10 1 0 10 0 0.6283
X14NC1 1 4 14 DELAY
G14 4 1 14 0 0.6283
R40C1 4 0 1.592
X40PC1 4 0 40 DELAY
G40 4 0 40 0 0.6283
X43PC2 4 3 43 DELAY
G43 4 3 43 0 1
R35 3 5 1.0
X56PC2 5 6 56 DELAY
G56 5 6 56 0 1
R46 4 6 1.0
X36NC2 3 6 36 DELAY
G36 6 3 36 0 1
X45NC2 4 5 45 DELAY
G45 5 4 45 0 1
*R35C2 3 5 15.9155
R46C2 4 6 15.9155
EVEN 6 0 4 0 1E6
EODD 5 0 3 0 1E6
********************
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5U
RDO 3 0 1K
.ENDS DELAY
********************
.AC LIN 1000 1 100K
.PRINT AC V(6) VP(6) V(5) VP(5) VDB(5) VDB(6)
.PROBE
.END
```

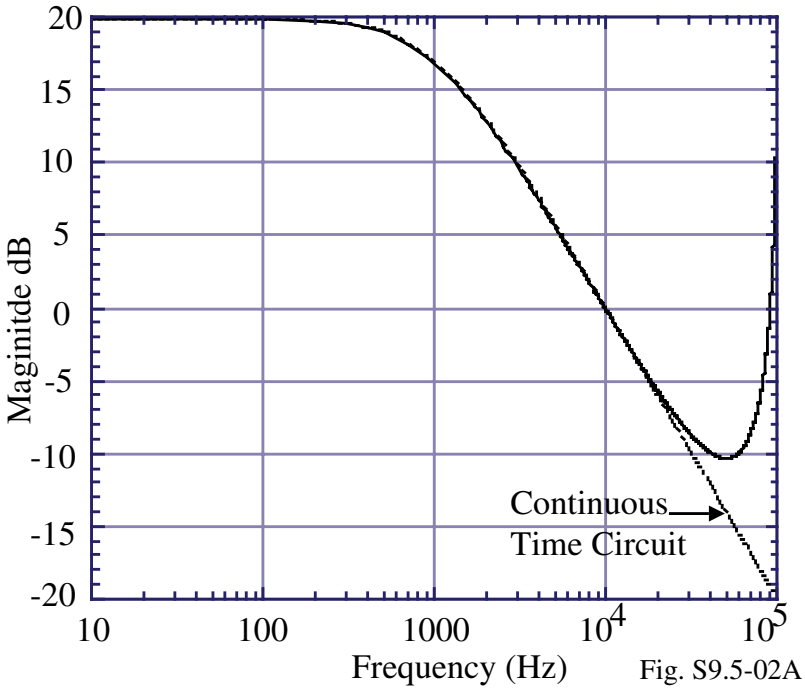


Fig. S9.5-02A

Problem 9.5-03

Repeat Ex. 9.5-1 for a first-order, lowpass circuit with a low frequency gain of +1 and a -3dB frequency of 5kHz.

Solution

TBD

Problem 9.5-04

Design a switched capacitor realization for a first-order , lowpass circuit with a low frequency gain of -10 and a -3dB frequency of 1kHz using a clock of 100kHz.

Solution

TBD

Problem 9.5-05

Design a switched capacitor realization for a first-order , highpass circuit with a high frequency gain of -10 and a -3dB frequency of 1kHz using a clock of 100kHz.

Solution

TBD

Problem 9.5-06

Repeat Ex. 9.5-2 for a treble boost circuit having 0dB gain from dc to 1kHz and an increase of gain at +20dB/dec. from 1kHz to 10kHz with a gain of +20dB from 10kHz and above (the mirror of the response of Fig. 9.5-7 around 1kHz).

Solution

TBD

Problem 9.5-07

The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (1.) Find the z-domain expression for $H^{oo}(z)$. (2.) Plot the magnitude and phase response of the switched capacitor circuit from 0 rps to the clock frequency (ω_c). Assume that the op amp is ideal for this problem. It may be useful to remember that Eulers formula is $e^{\pm jx} = \cos(x) \pm j\sin(x)$.

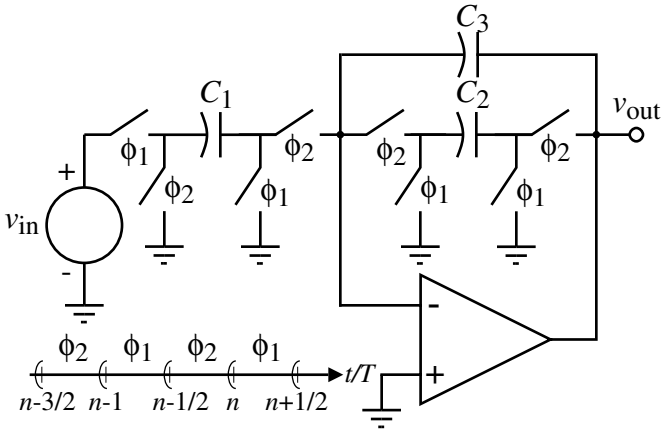
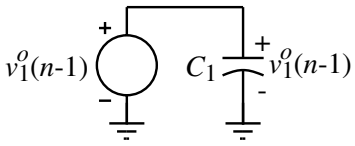


Figure P9.5-7

Solution

ϕ_1, $(n\text{-}1) \le t/T < (n\text{-}0.5)$:



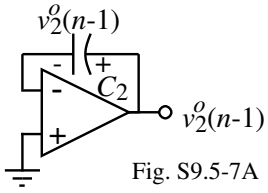


Fig. S9.5-7A

ϕ_2, $(n\text{-}0.5) \le t/T < (n)$:

From the equivalent circuit shown, we can write,

$$v_2^e(n\text{-}0.5) = v_2^o(n\text{-}1) - \frac{C_2}{C_3} v_2^e(n\text{-}0.5) + \frac{C_1}{C_3} v_1^o(n\text{-}1)$$

But, $v_2^o(n) = v_2^e(n\text{-}0.5) =$

$$v_2^o(n\text{-}1) - \frac{C_2}{C_3} v_2^o(n) + \frac{C_1}{C_3} v_1^o(n\text{-}1)$$

which gives,

$$V_2(z) = z^{-1}V_2(z) - \frac{C_2}{C_3} V_2(z) + \frac{C_1}{C_3} z^{-1}V_1(z)$$

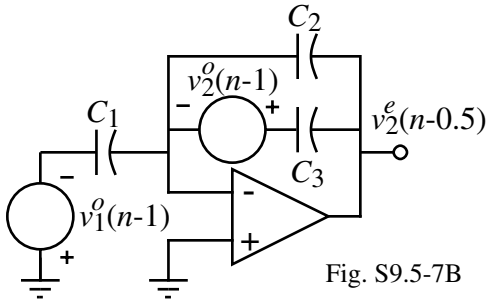


Fig. S9.5-7B

$$\therefore \quad \boxed{\frac{V_2(z)}{V_1(z)} = H^{oo}(z) = \frac{(C_1/C_3)z^{-1}}{1 + (C_2/C_3) - z^{-1}}} \quad \rightarrow \quad H^{oo}(e^{j\omega T}) = \frac{(C_1/C_3)e^{-j\omega T}}{1 + (C_2/C_3) - e^{-j\omega T}}$$

$$|H^{oo}(e^{j\omega T})| = \frac{0.2}{\sqrt{(1.1 - \cos\omega T)^2 + \sin^2\omega T}} \text{ and } \text{Arg}[H^{oo}(e^{j\omega T})] = -\omega T - \tan\text{-}1\left(\frac{\sin\omega T}{1.1\text{-}\cos\omega T}\right)$$

Replace ωT by $2\pi f/f_c$ and plot as a function of f/f_c to get the following plots.

Problem 9.5-08

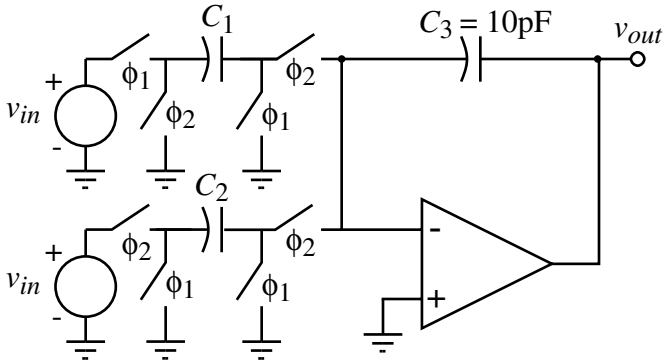
The switched capacitor circuit shown uses a two-phase, nonoverlapping clock. (a.) Find the z-domain expression for $H^{oo}(z)$. (b.) Use your expression for $H^{oo}(z)$ to design the values of C_1 and C_2 to achieve a realization to

$$H(s) = \frac{10{,}000}{s+1000}$$

if the clock frequency is 100kHz and C_3 = 10pF. Assume that the op amp is ideal.

Solution

(a.) Converting the problem into a summing integrator gives:



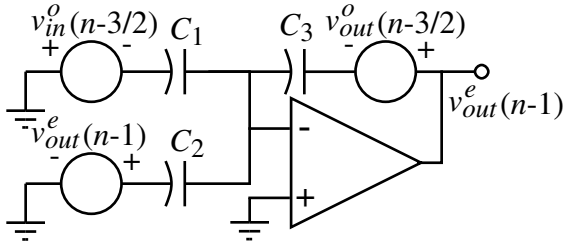
$\underline{\phi_1}$: $(n\text{-}1.5) \le t/T < (n\text{-}1)$

$v_{C1}^{o}(n\text{-}1.5) = v_{in}^{o}(n\text{-}1.5),\ v_{C2}^{o}(n\text{-}1.5) = 0$

and $v_{C3}^{o}(n\text{-}1.5) = v_{out}^{o}(n\text{-}1.5)$

$\underline{\phi_2}$: $(n\text{-}1) \le t/T < (n\text{-}0.5)$

The eq. circuit at t = 0+ is shown. ∴



$$v_{out}^{e}(n\text{-}1) = \frac{C_1}{C_3} v_{in}^{o}(n\text{-}1.5) - \frac{C_2}{C_3} v_{out}^{o}(n\text{-}0.5) + v_{out}^{o}(n\text{-}1.5)$$

$\underline{\phi_1}$: $(n\text{-}0.5) \le t/T < (n)$

$$v_{out}^{o}(n\text{-}0.5) = v_{out}^{e}(n\text{-}1) = \frac{C_1}{C_3} v_{in}^{o}(n\text{-}1.5) - \frac{C_2}{C_3} v_{out}^{o}(n\text{-}0.5) + v_{out}^{o}(n\text{-}1.5)$$

Transforming to the z-domain gives, $V_{out}^{o}(z) = z^{-1}\frac{C_1}{C_3} V_{in}^{o}(z) - \frac{C_2}{C_3} V_{out}^{o}(z) + z^{-1} V_{out}^{o}(z)$

Solving for $H^{oo}(z)$ gives, $\boxed{H^{oo}(z) = \frac{V_{out}^{o}(z)}{V_{in}^{o}(z)} = \frac{z^{-1}C_1}{C_2+C_3-C_3z^{-1}} = \frac{C_1}{z(C_2+C_3) - C_3}}$

(b.) Assume that $f \ll f_c$ and let $z \approx 1+sT$. Substituting into the above gives

$$H^{oo}(s) \approx \frac{C_1}{(1+sT)[C_2+C_3] - C_3} = \frac{C_1}{C_2+C_3-C_3+sT(C_2+C_3)} = \frac{C_1/C_2}{sT(C_2+C_3)/C_2 + 1}$$

Equating this result with the $H(s)$ in the problem statement gives

$$\frac{C_1}{C_2} = 10,\ \ 1+\frac{C_3}{C_2} = \frac{f_c}{1000} \Rightarrow \boxed{C_2 = C_3/99 = 10\text{pF}/99 = 0.101\text{pF}} \text{ and } \boxed{C_1 = 10C_2 = 1.01\text{pF}}$$

Problem 9.5-09

Find $H^{oo}(z)$ of the switched capacitor circuit shown.

Replace z by $e^{j\omega T}$ and identify the magnitude and phase response of this circuit.

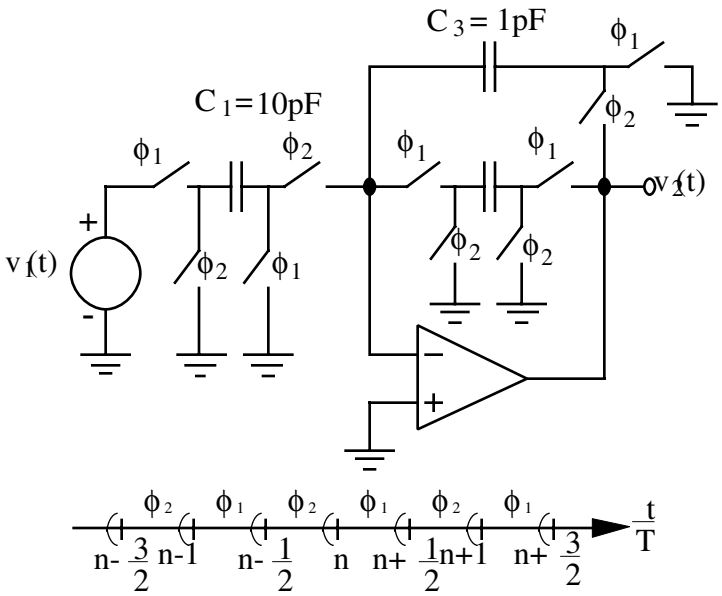


Figure P9.5-9

Solution

ϕ_2, $(n\text{-}0.5) \le t/T < (n)$:

With the ϕ_2 switches closed, the model is shown below.

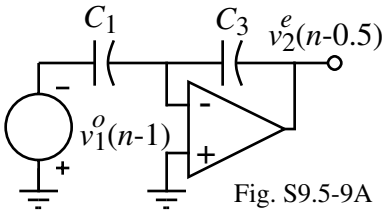


Fig. S9.5-9A

The output is given as,

$$v_2^e(n\text{-}0.5) = +\frac{C_1}{C_3} v_1^o(n\text{-}1)$$

ϕ_1, $(n) \le t/T < (n+0.5)$:

The model for this case is shown. The output is written as,

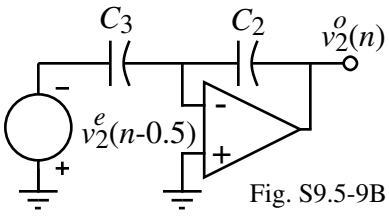


Fig. S9.5-9B

$$v_2^o(n) = +\frac{C_3}{C_2} v_2^e(n\text{-}0.5) = +\frac{C_3}{C_2}\cdot\frac{C_1}{C_3} v_1^o(n\text{-}1) = \frac{C_1}{C_2} v_1^o(n\text{-}1)$$

$$\therefore \quad V_2^o(z) = \frac{C_1}{C_3} z^{-1} V_1^o(z) \quad \rightarrow \quad \boxed{\frac{V_2^o(z)}{V_1^o(z)} = H^{oo}(z) = \frac{C_1}{C_2} z^{-1}}$$

$$\boxed{|H^{oo}(e^{j\omega T})| = \frac{C_1}{C_2} = 10} \quad \text{and} \quad \boxed{|\text{Arg}[H^{oo}(e^{j\omega T})] = -\omega T}$$

Comment: Note that this configuration is an amplifier that avoids taking the output of the op amp to zero when the feedback capacitor is shorted out. Therefore, slew rate limitation of the op amp is avoided.

Problem 9.5-10

The switched capacitor circuit shown is used to realize an audio bass-boost circuit. Find

$$H(e^{j\omega T}) = \frac{V_{out}(e^{j\omega T})}{V_{in}(e^{j\omega T})}$$

assuming that $f_c >> f_{signal}$. If $C_2 = C_4 = 1000$pF and $f_c = 10$kHz, find the value of C_1 and C_3 to implement the following transfer function.

$$\frac{V_{out}(s)}{V_{in}(s)} = -10\left(\frac{\frac{s}{100} + 1}{\frac{s}{10} + 1}\right)$$

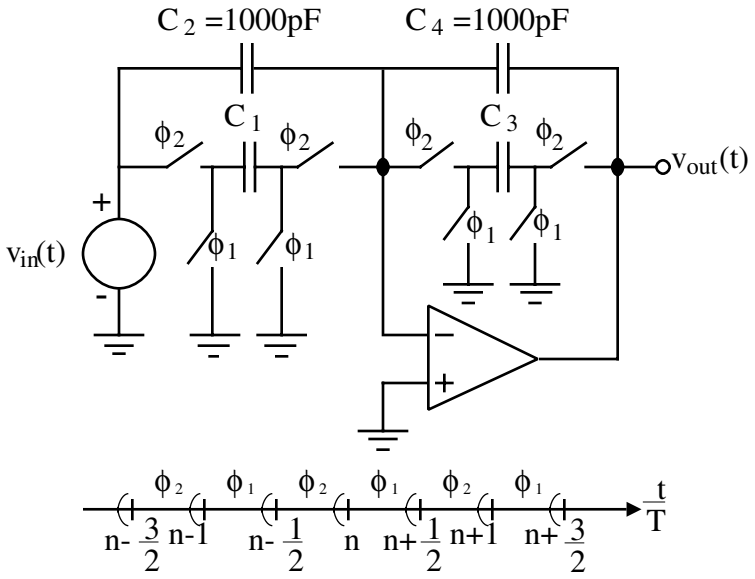
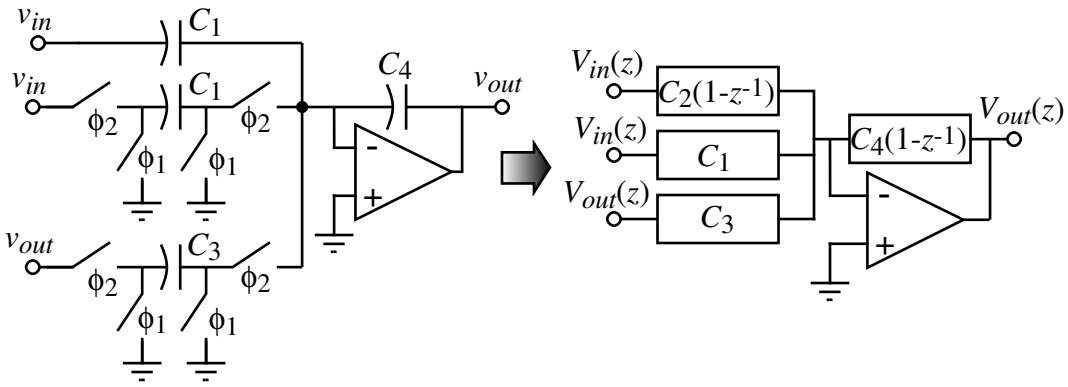


Figure P9.5-10

Solution

Write the circuit as the following summing integrator and replacing with *z*-domain models gives:



Summing currents gives,

$$C_2(1\text{-}z^{-1})V_{in}(z) + C_1V_{in}(z) + C_3V_{out}(z) + C_4(1\text{-}z^{-1})V_{out}(z) = 0$$

Transforming to the *s*-domain by $1\text{-}z^{-1} \approx \text{-}sT$ gives,

$$sT\,C_2\,V_{in}(s) + C_1V_{in}(s) + C_3V_{out}(s) + sT\,C_4\,V_{out}(s) = 0$$

$$\therefore\ H(s) = \frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{sT\,C_2+C_1}{sT\,C_4+C_3}\right) = -\left(\frac{C_1}{C_3}\right)\left(\frac{\frac{sT\,C_2}{C_1}+1}{\frac{sT\,C_4}{C_3}+1}\right) = -10\left(\frac{\frac{s}{100}+1}{\frac{s}{10}+1}\right)$$

Therefore, $\frac{C_1}{C_3} = 10$, $\frac{C_1}{TC_2} = 100$ and $\frac{C_3}{TC_4} = 10$

$$\therefore\ \boxed{C_1 = \frac{100C_2}{f_c} = \frac{100\cdot 1000\text{pF}}{10{,}000} = 10\text{pF}} \text{ and } \boxed{C_3 = 1\text{pF}}$$

Problem 9.6-01

Combine Figs. 9.6-2a and 9.6-2b to form a continuous time biquad circuit. Replace the negative resistor with an inverting op amp and find the s-domain frequency response. Compare your answer with Eq. (9.6-1).

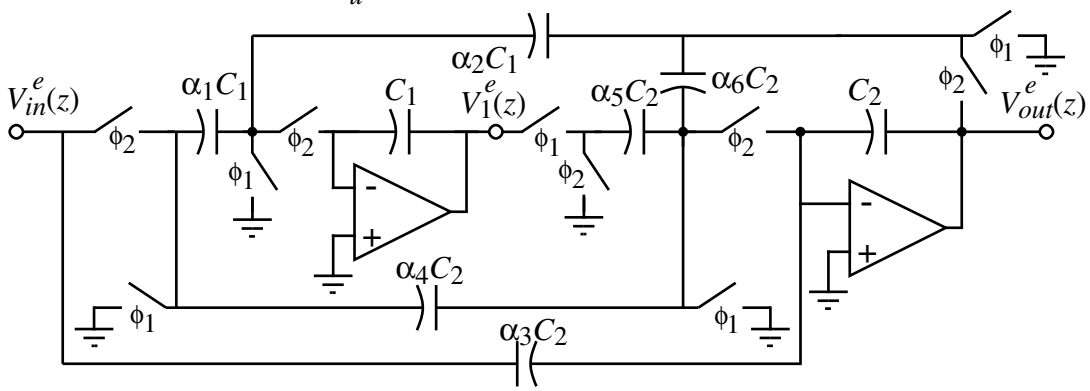
Solution

TBD

Problem 9.6-02

(a.) Use the low-Q switched capacitor biquad circuit shown to design the capacitor ratios of a lowpass second-order filter with a pole frequency of 1kHz, Q = 5 and a gain at dc of -10 if the clock frequency is 100kHz. What is the total capacitance in terms of C_u?

(b.) Find the clock frequency, f_c, that keeps all capacitor ratios less than 10:1. What is the total capacitance in terms of C_u for this case?



Design Eqs: $\alpha_1 = \dfrac{K_0 T}{\omega_o}$, $\alpha_2 = |\alpha_5| = \omega_o T$, $\alpha_3 = K_2$, $\alpha_4 = K_1 T$, and $\alpha_6 = \dfrac{\omega_o T}{Q}$.

Solution

(a.) $H(s) = \dfrac{-10\omega_o^2}{s^2 + \dfrac{\omega_o}{Q}s + \omega_o^2} \Rightarrow K_o = 10\omega_o^2, K_1 = K_2 = 0,\ \omega_o = 2000\pi$, and $Q = 5$

$\therefore \quad \alpha_1 = \dfrac{10\omega_o^2 T}{\omega_o} = 10\omega_o T$, $\alpha_2 = |\alpha_5| = \omega_o T$, $\alpha_3 = \alpha_4 = 0$, and $\alpha_6 = \dfrac{\omega_o T}{Q} = \dfrac{\omega_o T}{5}$

$\omega_o T = \dfrac{2\pi f_o}{f_c} = \dfrac{2\pi}{100} = 0.06283 \Rightarrow$ $\boxed{\alpha_1 = 0.6283,\ \alpha_2 = |\alpha_5|\ 0.06283,\ \alpha_6 = 0.01256}$

$$\boxed{\text{Total capacitance} = \frac{1}{0.6283} + \frac{1}{0.06283} + 2 + \frac{1}{0.01256} + \frac{1}{0.06283} = 115.45 C_u}$$

(b.) $\dfrac{\omega_o}{5f_c} = 0.1 \Rightarrow$ $\boxed{f_c = 2\omega_o = 4000\pi = 12.566\text{kHz}}$

Now, $\alpha_1 = 5$, $\alpha_2 = |\alpha_5| = 0.5$, and $a_6 = 0.1$

$$\boxed{\text{Total capacitance} = 5 + \frac{1}{.5} + 1 + \frac{1}{0.1} + \frac{1}{0.5} + 1 = 21 C_u}$$

Problem 9.6-03

A Tow-Thomas continuous time filter is shown. Give a discrete-time realization of this filter using strays-insensitive integrators. If the clock frequency is much greater than the filter frequencies, find the coefficients, a_i and b_i, of the following z-domain transfer function in terms of the capacitors of the discrete-time realization.

$$H(z) = \frac{a_0 + a_1 z^{-1} + a_2 z^{-2}}{b_0 + b_1 z^{-1} + b_2 z^{-2}}$$

Solution

The development of a discrete-time realization of the Tow-Thomas continuous time filter is shown to the right.

Using *z*-domain analysis, we can solve for the desired transfer function and find the coefficients.

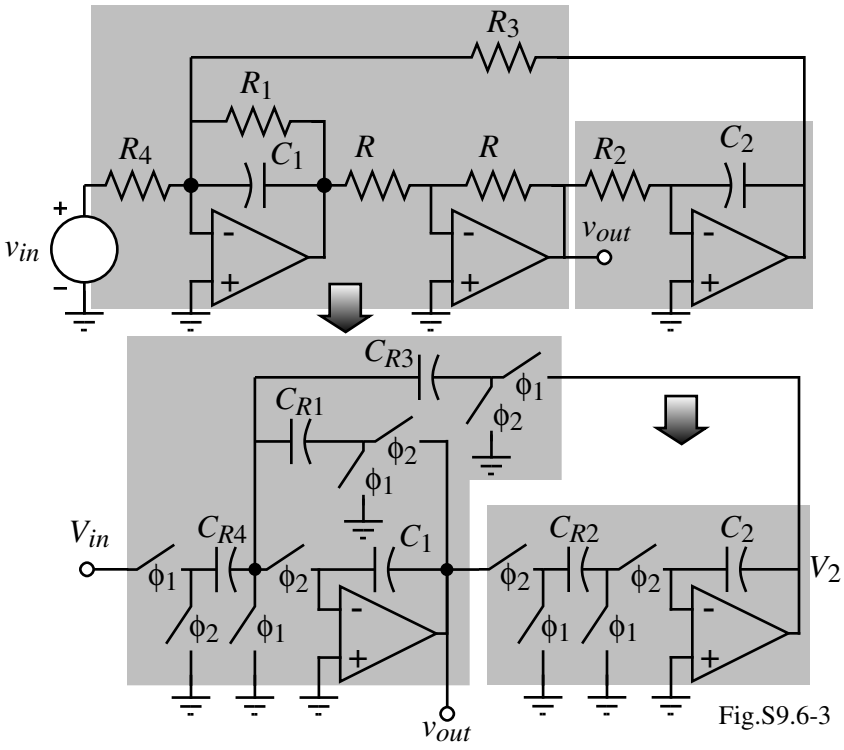


Fig.S9.6-3

$$V_{out}(z) = \frac{1}{1 - z^{-1}}\left[\frac{C_{R4}}{C_1}z^{-1}V_{in}(z) - \frac{C_{R1}}{C_1}z^{-1}V_{out}(z) + \frac{C_{R3}}{C_1}z^{-1}V_2(z)\right] \quad \text{and} \quad V_2(z) = -\frac{C_{R2}/C_2}{1 - z^{-1}}V_{out}(z)$$

$$\therefore \quad V_{out}(z) = \frac{1}{1 - z^{-1}}\left[\frac{C_{R4}}{C_1}z^{-1}V_{in}(z) - \frac{C_{R1}}{C_1}z^{-1}V_{out}(z) + \frac{C_{R2}C_{R3}}{C_1C_2}\frac{z^{-1}}{1 - z^{-1}}V_{out}(z)\right]$$

$$V_{out}(z)\left[(1 - z^{-1})^2 - \frac{C_{R1}}{C_1}(1 - z^{-1}) + \frac{C_{R2}C_{R3}}{C_1C_2}z^{-1}(1 - z^{-1})\right] = z^{-1}(1 - z^{-1})\frac{C_{R4}}{C_1}$$

$$\frac{V_{out}(z)}{V_{in}(z)} = H(z) = \frac{(z^{-1} - z^{-2})\frac{C_{R4}}{C_1}}{1 + 2z^{-1} + z^{-2} + \frac{C_{R1}}{C_1} - \frac{C_{R1}}{C_1}z^{-1} + \frac{C_{R2}C_{R3}}{C_1C_2}z^{-1} - \frac{C_{R2}C_{R3}}{C_1C_2}z^{-2}}$$

Equating coefficients gives,

$$a_0 = 0,\ a_1 = \frac{C_{R4}}{C_1},\ a_2 = -\frac{C_{R4}}{C_1},\ b_0 = 1 + \frac{C_{R1}}{C_1},\ b_1 = 2 - \frac{C_{R1}}{C_1} + \frac{C_{R2}C_{R3}}{C_1C_2} \text{ and } b_2 = 1 - \frac{C_{R2}C_{R3}}{C_1C_2}$$

Problem 9.6-04

Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = \frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1z + b_0}$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of second-order circuit is this?

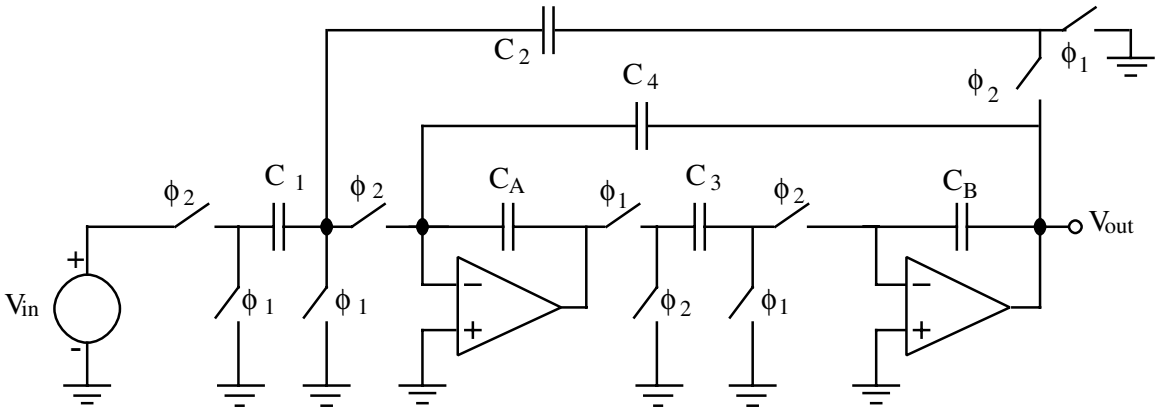


Figure P9.6-4

Solution

$$V_1(z) = \left(\frac{z}{z\text{-}1}\right)\frac{C_1}{C_A}V_{in}(z) - \left(\frac{z}{z\text{-}1}\right)\frac{C_2}{C_A}V_{out}(z) - \frac{C_4}{C_A}V_{out}(z) \quad \text{and} \quad V_{out}(z) = \left(\frac{1}{z\text{-}1}\right)\frac{C_3}{C_A}V_1(z)$$

Where $V_1(z)$ is the output of the first integrator. If $\alpha_{1A} = C_1/C_A$, $\alpha_{3B} = C_3/C_B$, $\alpha_{2A} = C_2/C_A$, and $\alpha_{4A} = C_4/C_A$ then we can write the following.

$$V_{out}(z) = \left(\frac{\alpha_{3B}}{z\text{-}1}\right)\left[-\frac{\alpha_{1A}z}{z\text{-}1}V_{in}(z) - \frac{\alpha_{2A}z}{z\text{-}1}V_{out}(z) - \alpha_{4A}V_{out}(z)\right]$$

$$\therefore \quad V_{out}(z)\left[1 + \frac{\alpha_{2A}\alpha_{3B}z}{(z\text{-}1)^2} + \frac{\alpha_{3B}\alpha_{4A}z}{z\text{-}1}\right] = \frac{\alpha_{1A}\alpha_{3B}z}{(z\text{-}1)^2}V_{in}(z)$$

$$H(z) = \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\alpha_{1A}\alpha_{3B}z}{(z\text{-}1)^2+\alpha_{2A}\alpha_{3B}z+(z\text{-}1)\alpha_{3B}\alpha_{4A}} = \boxed{\frac{-\alpha_{1A}\alpha_{3B}z}{z^2+(\alpha_{2A}\alpha_{3B}+\alpha_{3B}\alpha_{4A}\text{-}2)z+(1\text{-}\alpha_{3B}\alpha_{4A})}}$$

If $\omega T = sT << 1$, then $z \approx 1$ unless there are terms like $(z\text{-}1)$ in which case $z\text{-}1 \approx sT$. Therefore,

$$H(s) \approx \frac{-\alpha_{1A}\alpha_{3B}}{s^2T^2+sT\alpha_{3B}\alpha_{4A}+\alpha_{2A}\alpha_{3B}} = \frac{-\frac{\alpha_{1A}\alpha_{3B}}{T^2}}{s^2+s\frac{\alpha_{3B}\alpha_{4A}}{T}+\alpha_{2A}\alpha_{3B}} = \frac{-\frac{C_1C_3}{C_AC_B}\frac{1}{T^2}}{s^2+s\frac{C_3C_4}{C_BC_A}\frac{1}{T}+\frac{C_2C_3}{C_AC_B}}$$

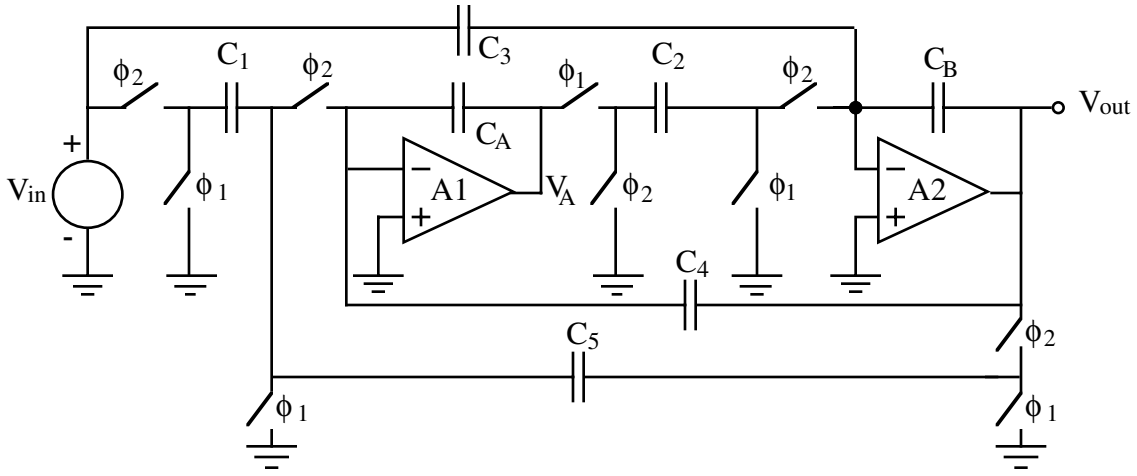
This circuit is a second-order bandpass transfer function.

Problem 9.6-05

Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = -\left[\frac{a_2z^2 + a_1z + a_0}{z^2 + b_1z + b_0}\right]$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of circuit is this?



Solution

For the output voltage of the first integrator, V_A, we can write,

$$V_A = f_1(V_A,V_{in},V_{out}) = \frac{-C_1}{C_A}\left(\frac{z}{z-1}\right)V_{in} - \frac{C_5}{C_A}\left(\frac{z}{z-1}\right)V_{out} - \frac{C_4}{C_A}V_{out}$$

Similarily for the output voltage of the second integrator, V_{out}, we can write,

$$V_{out} = f_2(V_A,V_{in}) = \frac{C_2}{C_B}\left(\frac{1}{z-1}\right)V_A - \frac{C_3}{C_B}V_{in}$$

Combining equations gives,

$$V_{out} = \frac{-z}{(z-1)^2}\left(\frac{C_2C_5}{C_AC_B}\right)V_{out} - \frac{z}{(z-1)^2}\left(\frac{C_1C_2}{C_AC_B}\right)V_{in} - \frac{1}{z-1}\left(\frac{C_2C_4}{C_AC_B}\right)V_{out} - \frac{C_3}{C_B}V_{in}$$

$$V_{out}\left[1 + \frac{z}{(z-1)^2}\left(\frac{C_2C_5}{C_AC_B}\right) + \frac{1}{z-1}\left(\frac{C_2C_4}{C_AC_B}\right)\right] = -\left[\frac{z}{(z-1)^2}\left(\frac{C_1C_2}{C_AC_B}\right) - \frac{C_3}{C_B}\right]V_{in}$$

$$V_{out}\left[(z-1)^2 + (z-1)\left(\frac{C_2C_4}{C_AC_B}\right) + z\left(\frac{C_2C_5}{C_AC_B}\right)\right] = -\left[(z-1)^2\frac{C_3}{C_B} + z\left(\frac{C_1C_2}{C_AC_B}\right)\right]V_{in}$$

$$\therefore \quad \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\left[\frac{C_3}{C_B}z^2 + \left(\frac{C_1C_2}{C_AC_B} - 2\frac{C_3}{C_B}\right)z + \frac{C_3}{C_B}\right]}{z^2 + \left(\frac{C_2(C_4+C_5)}{C_AC_B} - 2\right)z + \left(1 - \frac{C_2C_4}{C_AC_B}\right)} = -\left[\frac{a_2z^2+a_1z+a_0}{z^2+b_1z+b_0}\right]$$

Thus,

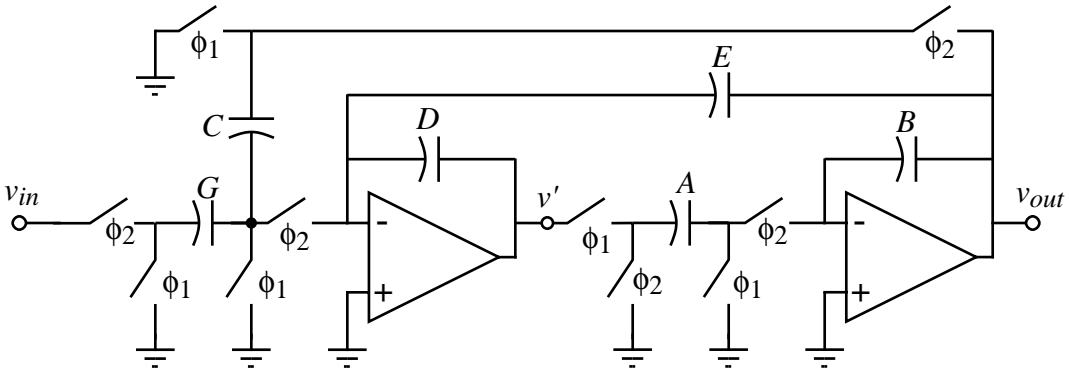
$$a_2=C_3/C_B,\ a_1=\frac{C_1C_2}{C_AC_B} - \frac{2C_3}{C_B},\ a_0=C_3/C_B,\ b_1=\frac{C_2(C_4+C_5)}{C_AC_B} - 2 \text{ and } b_0=1-\frac{C_2C_4}{C_AC_B}$$

Problem 9.6-06

Find the z-domain transfer function $H(z) = V_{out}(z)/V_{in}(z)$ in the form of

$$H(z) = -\left[\frac{a_2z^2 + a_1z + a_0}{z^2 + b_1z + b_0}\right]$$

for the switched capacitor circuit shown below. Evaluate the a_i's and b_i's in terms of the capacitors. Next, assume that $\omega T << 1$ and find H(s). What type of circuit is this? What is the pole frequency, ω_o, and pole Q?



Solution

$$V'(z) = -\left(\frac{G}{D}\right)\frac{z}{z-1}V_{in}(z) - \left(\frac{C}{D}\right)\frac{z}{z-1}V_{out}(z) - \left(\frac{E}{D}\right)V_{out}(z)$$

$$V_{out}(z) = \frac{A}{B}\frac{V'}{z-1} = \frac{A}{B}\frac{z}{z-1}\left[-\left(\frac{G}{D}\right)\frac{z}{z-1}V_{in}(z) - \left(\frac{C}{D}\right)\frac{z}{z-1}V_{out}(z) - \left(\frac{E}{D}\right)V_{out}(z)\right]$$

$$= -\frac{AG}{BD}\frac{z}{(z-1)^2}V_{in}(z) - \frac{AC}{BD}\frac{z}{(z-1)^2}V_{out}(z) - \frac{AE}{BD}\frac{V_{out}(z)}{z-1}$$

$$V_{out}(z)\left[1 + \frac{AE}{BD}\frac{1}{z-1} + \frac{AC}{BD}\frac{z}{(z-1)^2}\right] = -\frac{AG}{BD}\frac{z}{(z-1)^2}V_{in}(z)$$

$$\therefore \quad \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\frac{AG}{BD}z}{(z-1)^2 + \frac{AE}{BD}(z-1) + \frac{AC}{BD}z} \rightarrow \frac{V_{out}(z)}{V_{in}(z)} = \frac{-\frac{AG}{BD}z}{z^2 + \left(\frac{AE}{BD} + \frac{AC}{BD} - 2\right)z + \left(1 - \frac{AE}{BD}\right)}$$

Thus, $\boxed{a_2 = a_0 = 0,\ a_1 = \frac{AG}{BD},\ b_1 = \frac{AE}{BE} + \frac{AC}{BD} - 2, \text{ and } b_0 = 1 - \frac{AE}{BD}}$

Problem 9.6-07

The switched capacitor circuit shown below realizes the following z-domain transfer function

$$H(z) = -\left(\frac{a_2z^2 + a_1z + a_0}{b_2z^2 + b_1z + 1}\right)$$

where

$C_6=a_2/b_2$, $C_5=(a_2-a_0)/b_2C_3$, $C_1=\frac{a_0+a_1+a_2}{b_2C_3}$, $C_4=\frac{1-(b_0/b_2)}{C_3}$ and $C_2C_3 = \frac{1+b_1+b_2}{b_2}$. Design a switched capacitor realization for the function

$$H(s) = \frac{-10^6}{s^2 + 100s + 10^6}$$

where the clock frequency is 10 kHz. Use the bilinear transformation, $s = (2/T)[(z-1)/(z+1)]$, to map $H(s)$ to $H(z)$. Choose $C_2 = C_3$ and assume that $C_A = C_B = 1$.

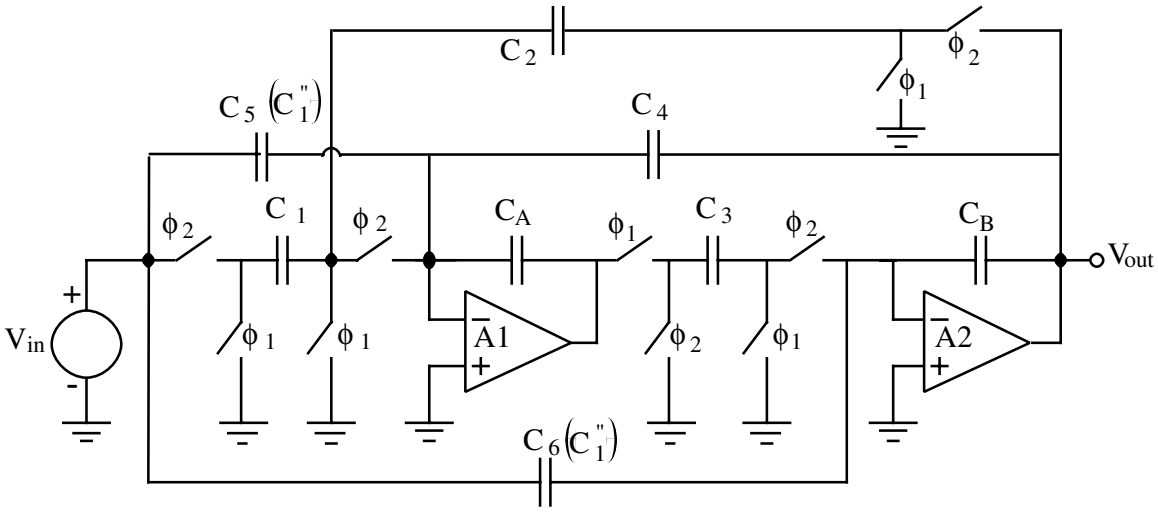


Figure P9.6-7

Solution

Apply the bilinear transformation

$$s = \frac{2}{T}\left(\frac{z-1}{z+1}\right) = 2\text{x}10^4\left(\frac{z-1}{z+1}\right)$$

to $H(s)$ to get,

$$H(z) = \frac{-10^6}{4\text{x}10^8\left(\frac{z-1}{z+1}\right)^2+200\text{x}10^4\left(\frac{z-1}{z+1}\right)\left(\frac{z+1}{z+1}\right)+10^6\left(\frac{z+1}{z+1}\right)^2}$$

$$= \frac{-10^6(z^2+2z+1)}{4\text{x}10^8(z^2-2z+1)+2\text{x}10^6(z^2-1)+10^6(z^2+2z+1)}$$

$$= \frac{-(10^6z^2+2\text{x}10^6z+10^6)}{(4\text{x}10^8+2\text{x}10^6+10^6)z^2+(-8\text{x}10^8+2\text{x}10^6)z+(4\text{x}10^8-2\text{x}10^6+10^6)}$$

Problem 9.6-07 - Continued

$$= \frac{-(10^6 z^2+2\text{x}10^6 z+10^6)}{4.03\text{x}10^8 z^2-7.98\text{x}10^8 z+3.99\text{x}10^8} = \frac{-(0.002506z^2+0.005013z+0.002506)}{1.010025z^2-2.0000z+1}$$

Now equating to the coefficients,

$$C_6 = \frac{a_2}{b_2} = \frac{0.002506}{1.010025} = 0.002481,\ C_5 = \frac{a_2-a_0}{b_2 C_3} = 0,$$

$$C_2 C_3 = \frac{1+b_1+b_2}{b_2} = \frac{1+(-2)+1.010025}{1.010025} = 0.009925 \quad \Rightarrow C_2 = C_3 = 0.099627$$

$$C_1 = \frac{a_0+b_1+b_2}{b_2 C_3} = \frac{0.002506+0.005013+0.002506}{1.010025 \cdot 0.0099627} = 0.099633$$

$$C_4 = \frac{1+(b_0/b_2)}{C_3} = \frac{1-(1/1.010025)}{0.099627} = 0.099627$$

$\therefore$ $\boxed{C_1=0.099633,\ C_2=C_3=0.099627,\ C_4=0.099627,\ C_5=0,\ C_6=0.002481}$

$C_{max}/C_{min} = 1/0.002625 = \underline{\underline{403.06}}$

Normalize all capacitors by 0.002625 to get

$\Sigma C_\mu = [(403.6)2+(37.953)2+37.953+37.955+1] = \underline{\underline{958.9C_\mu}}$

Problem 9.7-01

Find the minimum order of a Butterworth and Chebyshev filter approximation to a filter with the specifications of T_{PB} = -3dB, T_{SB} = -40dB, and Ω_n = 2.0.

Solution

For the Butterworth approximation, use Eq. (9.7-7) and for the Chebyshev approximation use Eq. (9.7-12), both with ε = 1. The results are shown below.

N	T_{SB}(dB) = $-10log_{10}(1+2^{2N})$	T_{SB}(dB) = $-10log_{10}[1+cosh^2(Ncosh^{-1}2)]$
1	-6.99 dB	-6.99 dB
2	-12.30 dB	-16.99 dB
3	-18.13 dB	-28.31 dB
4	-24.10 dB	-39.74 dB
5	-30.11 dB	-51.17 dB
6	-36.12 dB	
7	-42.14 dB	

The minimum order for the Butterworth is 7 while the minimum order for the Chebyshev i 5 and in many cases 4 would work.

Problem 9.7-02

Find the transfer function of a fifth-order, Butterworth filter approximation expressed as products of first- and second-order terms. Find the pole frequency, ω_p and the Q for each second-order term.

Solution

From Table 9.7-1 we get,

$$T(s) = \frac{1}{(s+1)(s^2+0.61804s+1)(s^2+1.84776s+1)}$$

The pole frequency and Q for a general second order term of (s^2+a_1s+1) is

$$\omega_p = 1 \text{ and } Q = \frac{1}{a_1}$$

For both second order terms, the pole frequency is 1 radian/sec.

For the first second-order term, the $Q = 1.61804$.

For the second, second-order term, the $Q = 0.541196$.

Problem 9.7-03

Redesign the second stage of Ex. 9.7-5 using the high-Q biquad and find the total capacitance required for this stage. Compare with the example.

Solution

$$T_{n2}(s_n) = \frac{0.9883}{s_n^2 + 0.1789 s_n + 0.9883} \qquad \Rightarrow \qquad \omega_{n2} = 0.9941 \text{ and } Q_2 = 5.557$$

For the lowpass high-Q biquad, $K_1 = K_2 = 0 \;\Rightarrow\; \alpha_{32} = \alpha_{62} = 0$ and $K_0 = \omega_{n2}^2$

$$\therefore \qquad \alpha_{22} = |\alpha_{52}| = \omega_{n2} T_n = 0.9941 \frac{\omega_{PB}}{f_c} = \underline{\underline{0.3123}}$$

$$\alpha_{12} = \frac{\omega_{n2}^2 T_n}{\omega_{n2}} = \omega_{n2} T_n = \underline{\underline{0.3123}}$$

$$\alpha_{42} = \frac{1}{Q} = \underline{\underline{0.1800}}$$

Schematic of the second-stage:

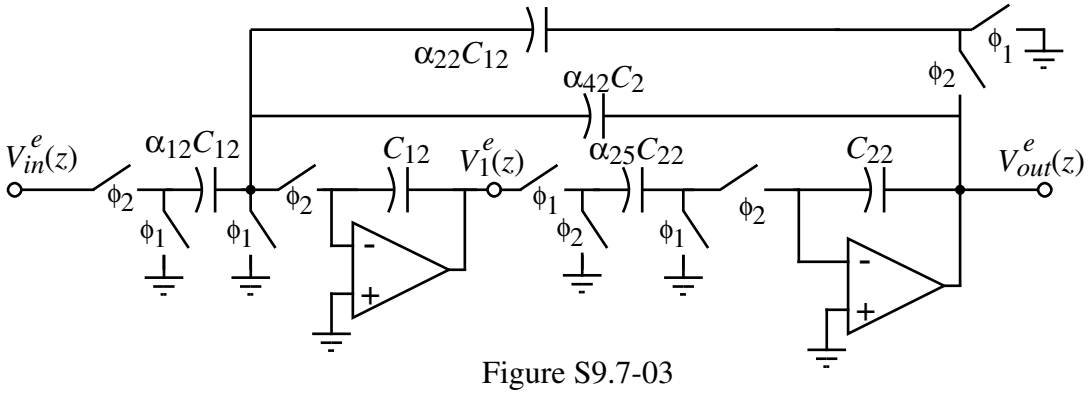


Figure S9.7-03

Total capacitance is:

$$\Sigma C = \left(1 + \frac{2(0.3123)}{0.1880} + \frac{1}{0.1800}\right) + \left(1 + \frac{1}{0.3123}\right) = 10.027 + 4.202 = \underline{\underline{14.229 C_\mu}}$$

Note that this value is 17.32 when a low-Q stage is used.

Problem 9.7-04

Design a cascaded, switched capacitor, 5th-order, lowpass filter using the cascaded approach based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{1}{(s_n+1)(s_n^2+0.61804s_n+1)(s_n^2+1.61804s_n+1)}$$

The passband of the filter is to 1000Hz. Use a clock frequency of 100kHz and design each stage giving the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio, and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

Stage 1, First-Order Stage (Use Fig. 9.5-1):

$$T_1(s_n) = \frac{\alpha_{11}/\alpha_{21}}{(s_nT_n/\alpha_{21})+1} = \frac{1}{s_n+1} \quad \Rightarrow \quad \alpha_{11} = \alpha_{21} \quad \text{and} \quad \alpha_{21} = T_n$$

$$\alpha_{11} = \alpha_{21} = T_n = \frac{\omega_{PB}}{f_c} = \frac{2000\pi}{100{,}000} = \underline{\underline{0.06283}}$$

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.06283} = \underline{\underline{15.92}} \quad \text{and} \quad \Sigma C = 2 + \frac{1}{0.06283} = \underline{\underline{19.92C_u}}$$

Stage 2, Second-order Stage (Use Low-Q Lowpass Biquad):

$$T_2(s_n) = \frac{1}{s_n^2+1.61804s_n+1} \quad \Rightarrow \quad \omega_{n2} = 1 \text{ rad/sec and } Q_2 = 0.61804$$

From the low-Q biquad relationships, $K_1 = K_2 = 0 \quad \Rightarrow \quad \alpha_{32} = \alpha_{42} = 0$

$$\alpha_{22} = |\alpha_{52}| = \omega_nT_n = \underline{\underline{0.06283}} \quad \text{and} \quad \alpha_{62} = \frac{\omega_nT_n}{Q_2} = \frac{0.06283}{0.61804} = \underline{\underline{0.1017}}$$

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.1017} = \underline{\underline{9.837}}$$

$$\text{and} \quad \Sigma C = \left(2 + \frac{1}{0.06283}\right) + \left(\frac{1}{0.06283} + \frac{0.1017}{0.06283} + 1\right) = \underline{\underline{36.45C_u}}$$

Stage 3, Second-order Stage (Use Low-Q Lowpass Biquad):

$$T_3(s_n) = \frac{1}{s_n^2+0.61804s_n+1} \quad \Rightarrow \quad \omega_{n2} = 1 \text{ rad/sec and } Q_2 = 1.6180$$

From the low-Q biquad relationships, $K_1 = K_2 = 0 \quad \Rightarrow \quad \alpha_{33} = \alpha_{43} = 0$

$$\alpha_{23} = |\alpha_{53}| = \omega_nT_n = \underline{\underline{0.06283}} \quad \text{and} \quad \alpha_{62} = \frac{\omega_nT_n}{Q_2} = \frac{0.06283}{1.6180} = \underline{\underline{0.0391}}$$

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.0391} = \underline{\underline{25.59}}$$

$$\text{and} \quad \Sigma C = \left(2 + \frac{1}{0.06283}\right) + \left(\frac{1}{0.0391} + \frac{0.06283}{0.0391} + 1\right) = \underline{\underline{46.10C_u}}$$

Problem 9.7-04 – Continued

Schematic:

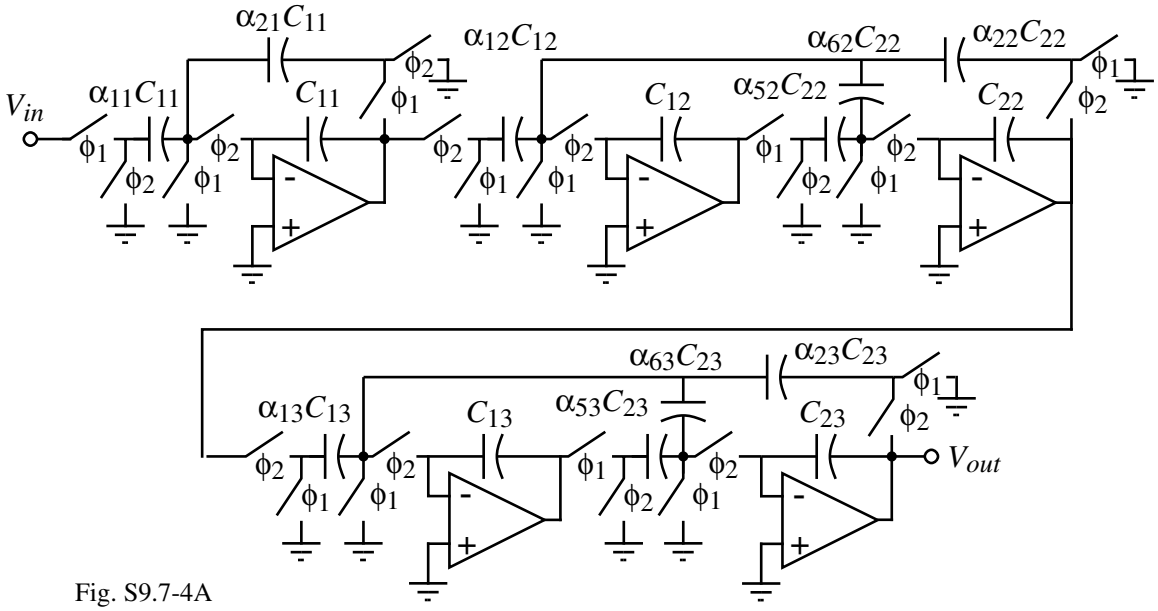


Fig. S9.7-4A

SPICE File:

```
*** HW9 PROBLEM2 (Problem 9.7-4) ***
*** Node 21 and 22 are outputs
VIN 1 0 DC 0 AC 1
*** STAGE1 ***
XNC11 1 2 3 4 NC1
XUSCP11 3 4 5 6 USCP
XPC21 5 6 3 4 PC1
XAMP11 3 4 5 6 AMP
*** STAGE2 ***
XPC12 5 6 7 8 PC1
XUSCP12 7 8 9 10 USCP
XPC22 7 8 13 14 PC1
XAMP12 7 8 9 10 AMP
XNC52 9 10 11 12 NC1
XUSCP22 11 12 13 14 USCP
XPC62 11 12 13 14 PC2
XAMP22 11 12 13 14 AMP
*** STAGE3 ***
XPC13 13 14 15 16 PC1
XPC23 15 16 21 22 PC1
XUSCP43 15 16 21 22 USCP1
XUSCP13 15 16 17 18 USCP
XAMP13 15 16 17 18 AMP
XNC53 17 18 19 20 NC1
XUSCP23 19 20 21 22 USCP
XAMP23 19 20 21 22 AMP
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
```

Problem 9.7-05

Repeat Problem 9.7-3 for a 5th-order, highpass filter having the same passband frequency. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

Problem 9.7-06

Repeat Problem 9.7-3 for a 5th-order, bandpass filter having center frequency of 1000Hz and a -3dB bandwidth of 500Hz. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

Problem 9.7-07

Design a switched capacitor 6th-order, bandpass filter using the cascaded approach and based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{2}{(s_n+1)(s_n^2+2s_n+2)}$$

The center frequency of the bandpass filter is to be 1000Hz with a bandwidth of 100Hz. Use a clock frequency of 100kHz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

Problem 9.7-08

Design a switched capacitor, third-order, highpass filter based on the lowpass normalized prototype transfer function of Problem 9.7-7. The cutoff frequency (f_{PB}), is to be 1000Hz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

TBD

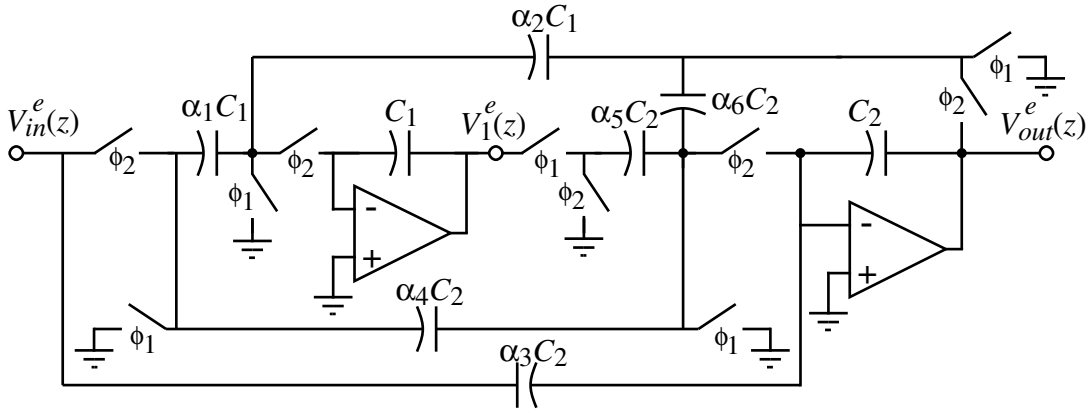
Problem 9.7-09

Design a switched capacitor, third-order, highpass filter based on the following lowpass, normalized prototype transfer function.

$$H_{lpn}(s_n) = \frac{0.5({s_n}^2+4)}{(s_n+1)({s_n}^2+2s_n+2)}$$

The cutoff frequency (f_{PB}), is to be 1000Hz. Use a clock frequency of 100kHz. Design each stage given the capacitor ratios as a function of the integrating capacitor (the unswitched feedback capacitor around the op amp), the maximum capacitor ratio and the units of normalized capacitance, C_u. Give a schematic of your realization connecting your lowest Q stages first. Use the low-Q biquad given below for the second-order stage. The approximate s-domain transfer function for the low-Q biquad is,

$$H^{ee}(s_n) = \frac{-\left[\alpha_3 {s_n}^2 + \frac{s_n\alpha_4}{T_n} + \frac{\alpha_1\alpha_5}{{T_n}^2}\right]}{{s_n}^2 + \frac{s_n\alpha_6}{T_n} + \frac{\alpha_2\alpha_5}{{T_n}^2}}$$



Low Q, switched capacitor, biquad realization.

Solution

Perform a normalized lowpass to normalized highpass transformation:

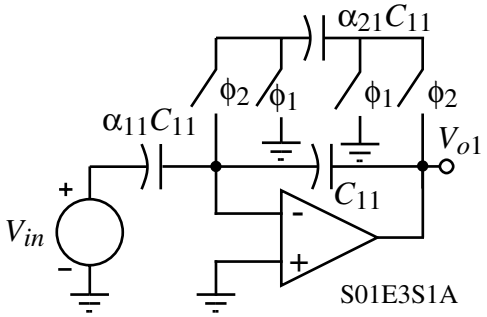
$$H_{hpn}(s_n) = \frac{0.5\left(\frac{1}{{s_n}^2}+4\right)}{\left(\frac{1}{s_n}+1\right)\left(\frac{1}{{s_n}^2}+\frac{2}{s_n}+2\right)} = \frac{0.5s_n(4{s_n}^2+1)}{(s_n+1)(1+2s_n+2{s_n}^2)} = \left(\frac{s_n}{s_n+1}\right)\left(\frac{{s_n}^2+0.25}{{s_n}^2+s_n+0.5}\right)$$

First-order stage design:

Equating currents at the inverting input of the op amp gives,

$$\alpha_{11}(1-z^{-1})V_{in}^{e}(z) + \alpha_{21}V_{o1}^{e}(z) + (1-z^{-1})V_{o1}^{e}(z) = 0$$

Solving for the $H^{ee}(z)$ tranfer function gives,



Problem 9.7-09 - Continued

$$H^{ee}(z) = \frac{V_{o1}^{e}(z)}{V_{in}^{e}(z)} = \frac{-\alpha_{11}(1-z^{-1})}{\alpha_{21} + (1-z^{-1})} \quad \rightarrow \quad H^{ee}(s_n) \approx \frac{V_{o1}^{e}(s_n)}{V_{in}^{e}(s_n)} = \frac{-\alpha_{11}s_nT_n}{\alpha_{21}+s_nT_n} = \frac{-\alpha_{11}s_n}{s_n + \frac{\alpha_{21}}{T_n}}$$

Equating with the normalized highpass transfer function gives,

$$\alpha_{11} = \underline{1} \text{ and } \alpha_{21} = T_n = \frac{\omega_{PB}}{f_c} = \frac{2000\pi}{100{,}000} = \underline{\underline{0.06283}}$$

$$\Sigma C_\mu = \frac{2}{0.06283} + 1 = 32.832C_\mu$$

Next, consider the second-order stage design:

Equating $H^{ee}(s)$ with $\left(\frac{s_n^2+0.25}{s_n^2+s_n+0.5}\right)$ gives,

$$\alpha_{32} = \underline{1},\ \alpha_{42} = \underline{0},\ \alpha_{12}\alpha_{52} = 0.25T_n^2,\ \alpha_{62}=T_n = \frac{2000\pi}{100{,}000} = \underline{\underline{0.06823}} \text{ and } \alpha_{22}\alpha_{52} = \frac{T_n^2}{2}$$

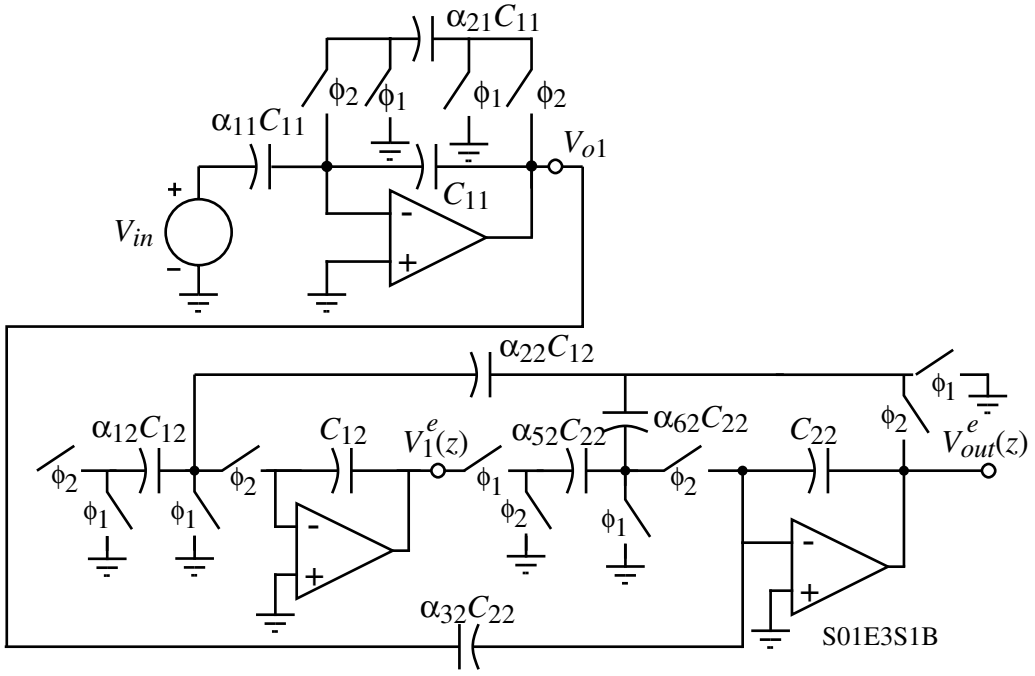
Let $\alpha_{22} = \alpha_{52}$, then $\alpha_{22} = \alpha_{52} = \frac{T_n}{\sqrt{2}} = \frac{\omega_{PB}}{\sqrt{2}f_c} = \frac{2000\pi}{\sqrt{2}\ 100{,}000} = \underline{\underline{0.04443}}$

Therefore, $\alpha_{12} = \frac{T_n^2}{4\alpha_{52}} = \frac{\sqrt{2}T_n}{4} = \underline{\underline{0.02221}}$

$$\Sigma C_\mu = \left[\left(1 + \frac{0.04443}{0.2221} + \frac{1}{0.02221}\right) + \left(1 + \frac{0.06283}{0.04443} + \frac{2}{0.04443}\right)\right] = 48.025+47.4287$$

Total $\Sigma C_\mu = 32.832 + 48.025 + 47.429 = \underline{\underline{127.84C_\mu}}$ $C_{max}/C_{min} = 1/0.02221 = \underline{\underline{45.025}}$

Filter schematic:



Problem 9.7-09 – Continued

```
.SUBCKT NC1 1 2 3 4
RNC1 1 0 15.916
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.06283
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.06283
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.06283
RNC2 4 0 15.916
.ENDS NC1
.SUBCKT PC1 1 2 3 4
RPC1 2 4 15.916
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 9.8328
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT USCP1 1 2 3 4
R1 1 3 1.6181
R2 2 4 1.6181
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 0.6180
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 0.6180
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 0.6180
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 0.6180
.ENDS USCP1
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 1000 10 99K
.PROBE
.END
```

Problem 9.7-10

Write the minimum set of state equations for each of the circuits shown below. Use voltage analogs of current (R=1Ω). The state equations should be in the form of the state variable equal to other state variables, including itself.

Solution

(a) $$V_1 = \frac{1}{s_n C_{1n}}\left[\frac{V_{in}}{R_{0n}} - \frac{V_1}{R_{0n}} - V_2'\right]$$

$$V_2' = \frac{1}{s_n L_{2n}}(V_1 - V_{out})$$

$$V_{out} = \frac{1}{s_n C_{3n}}\left[V_2' - \frac{V_{out}}{R_{4n}} - \frac{V_1}{R_{0n}}\right]$$

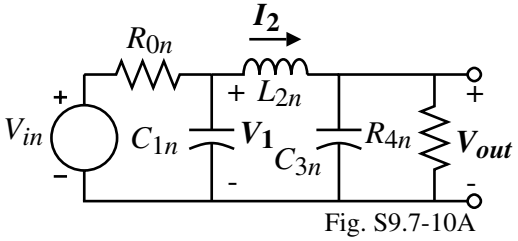


Fig. S9.7-10A

$$\therefore \quad V_1' = \frac{1}{s_n L_{1bn} + \frac{1}{s_n C_{1n}}}[V_1 - V_{out}]$$

$$= \frac{\frac{s_n}{L_{1bn}}}{s_n^2 + 1}[V_1 - V_{out}]$$

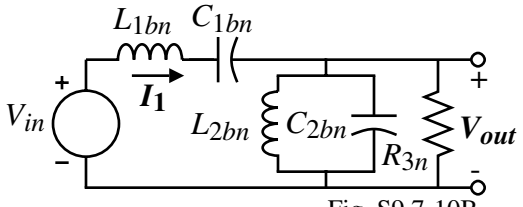


Fig. S9.7-10B

$$V_{out} = \frac{1}{s_n C_{2bn} + \frac{1}{s_n L_{2bn}}}\left(V_1' - \frac{V_{out}}{R_{4n}}\right) = \frac{\frac{s_n}{C_{2bn}}}{s_n^2 + 1}\left(V_1' - \frac{V_{out}}{R_{4n}}\right)$$

$\therefore$ The simplest way to work this one is make the following transformation (see pp. 228-230 of *Switched Capacitor Circuits*, P.E. Allen and E.S. Sanchez, Van Nostrand Reinhold,1984).

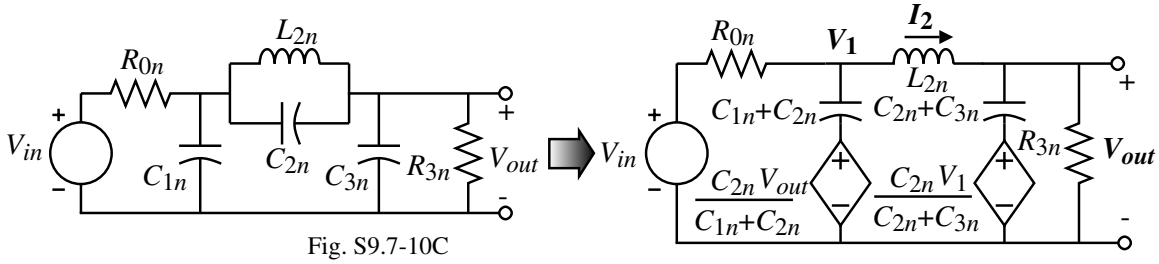


Fig. S9.7-10C

$$V_1 = \frac{1}{s_n(C_{1n} + C_{2n})}\left[\frac{V_{in}}{R_{0n}} - \frac{V_1}{R_{0n}} - V_2'\right] + \frac{C_{2n}}{C_{1n} + C_{2n}} V_{out}$$

$$V_2' = \frac{1}{s_n L_{2n}}(V_1 - V_{out})$$

$$V_{out} = \frac{1}{s_n(C_{2n} + C_{3n})}\left[V_2' - \frac{V_{out}}{R_{3n}}\right] + \frac{C_{2n}}{C_{2n} + C_{3n}} V_{out}$$

Problem 9.7-11

Give a continuous time and switched capacitor implementation of the following state equations. Use minimum number of components and show the values of the capacitors and the phasing of each switch (ϕ_1 and ϕ_2). Give capacitor values in terms of the parameters of the state equations and Ω_n and f_c for the switched capacitor implementations.

1.) $V_1 = \frac{1}{sK}[-\alpha_1 V_1 + \alpha_2 V_2 - \alpha_3 V_3]$

2.) $V_1 = \frac{s}{s^2+1}[-\alpha_1 V_1 + \alpha_2 V_2 - \alpha_3 V_3]$

$\therefore \quad V_1 = \frac{1}{sK}[-\alpha_1 V_1 + \alpha_2 V_2] + \alpha_3 V_3$

Solution

1.)

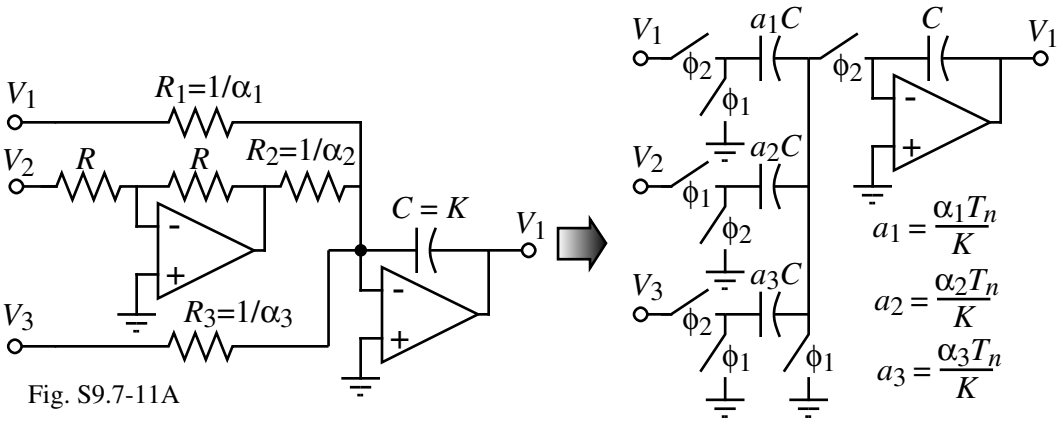


Fig. S9.7-11A

2.)

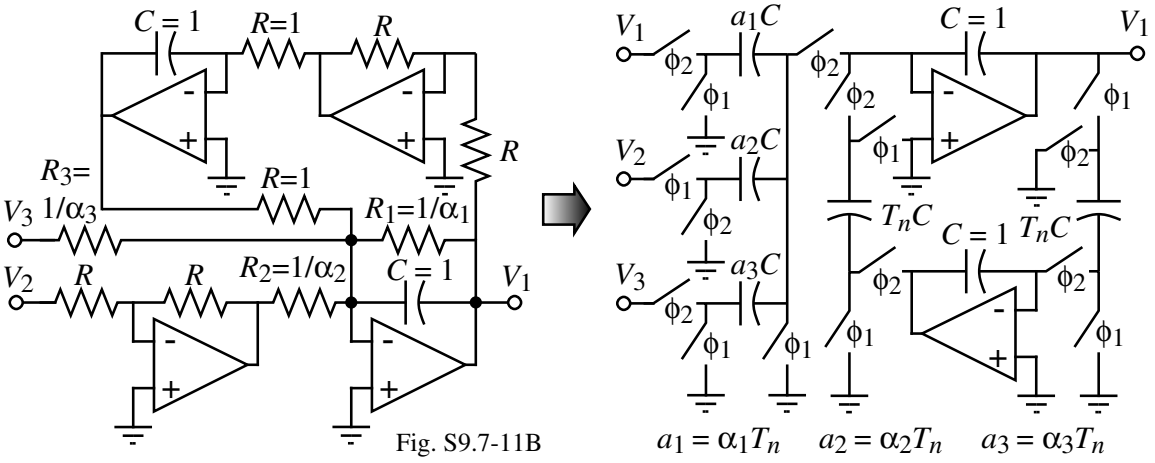


Fig. S9.7-11B

Problem 9.7-11 - Continued

3.)

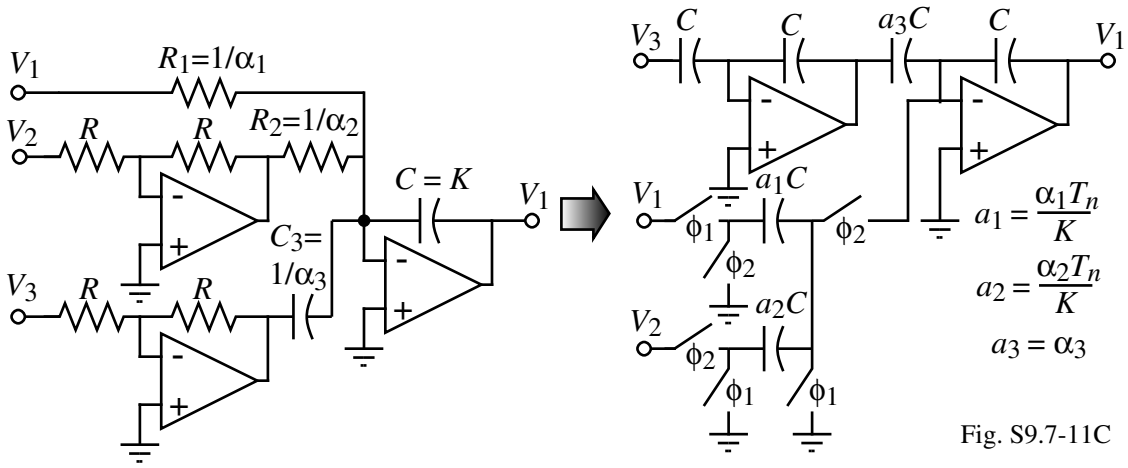


Fig. S9.7-11C

Problem 9.7-12

Find a switched capacitor, realization of the low-pass normalized RLC ladder filter shown. The cutoff frequency of the low-pass filter is 1000Hz and the clock frequency is 100kHz. Give the value of all capacitors in terms of the integrating capacitor of each stage and show the correct phasing of switches. What is the C_{max}/C_{min} and the total units of capacitance for this filter? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

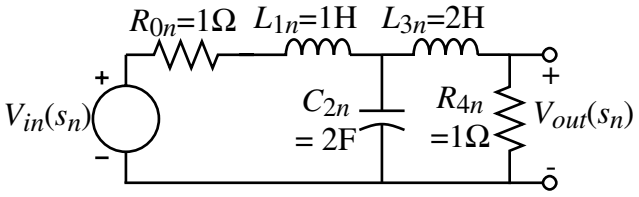


Figure P9.7-12

Solution

The state equations are:

$$V_s = I_1R_{on}+sL_{1n}I_1+V_2 \rightarrow I_1 = \frac{1}{sL_{1n}}\left(V_s - \frac{RI_1R_{on}}{R} - V_2\right) \rightarrow \boxed{V_1' = \frac{R}{sL_{1n}}\left(V_s - \frac{V_1'R_{on}}{R} - V_2\right)}$$

$$I_1 - I_3 = sC_{2n}V_2 \;\rightarrow\; V_1' - V_3' = sRC_{2n}V_2 \;\rightarrow\; \boxed{V_2 = \frac{1}{sRC_{2n}}(V_1' - V_3')}$$

$$V_2 = sL_{3n}I_3 + I_3R_{4n} \;\rightarrow\; I_3 = \frac{1}{sL_{3n}}(V_2 - I_3R_{4n}) \;\rightarrow\; V_3' = \frac{R}{sL_{3n}}\left(V_2 - \frac{R_{4n}}{R}V_3'\right)$$

But, $V_{out} = I_3R_{4n} = V_3'\frac{R_{4n}}{R} \rightarrow V_3' = \frac{R}{R_{4n}}V_{out} \rightarrow \boxed{V_{out} = \frac{R_{4n}}{sL_{3n}}(V_2 - V_{out})}$

Normalized realizations:

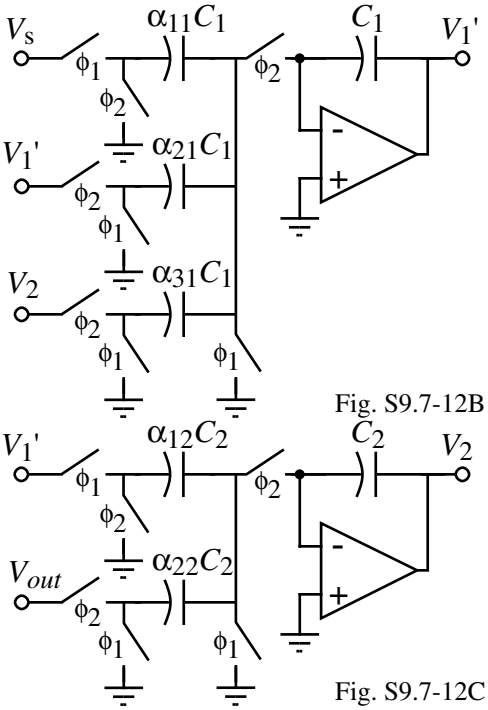


Fig. S9.7-12B

Fig. S9.7-12C

$$V_1' \approx \frac{1}{sT_n}[\alpha_{11}V_s - \alpha_{21}V_1' - \alpha_{31}V_2]$$

Comparing with the first state equation:

$$\frac{\alpha_{11}}{T_n} = \frac{R}{L_{1n}} \;\rightarrow\; \alpha_{11} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n}{f_cL_{1n}} = \frac{1\cdot 2000\pi}{10^5\cdot 1}$$

$$\alpha_{11} = \pi/50 = \underline{\underline{0.0628}} = \alpha_{21}$$

$$\frac{\alpha_{31}}{T_n} = \frac{R_{on}}{L_{1n}} \;\rightarrow\; \alpha_{31} = \frac{R_{on}\Omega_n}{f_cL_{1n}} = \alpha_{11} = \underline{\underline{0.0628}}$$

$$V_2 \approx \frac{1}{sT_n}[\alpha_{12}V_1' - \alpha_{22}V_{out}]$$

Comparing with the second state equation:

$$\frac{\alpha_{12}}{T_n} = \frac{1}{RC_{2n}} \;\rightarrow\; \alpha_{12} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n}{Rf_cC_{2n}} = \frac{1\cdot 2000\pi}{1\cdot 2\cdot 10^5}$$

$$\alpha_{12} = \pi/100 = \underline{\underline{0.0314}} = \alpha_{22}$$

Problem 9.7-12 – Continued

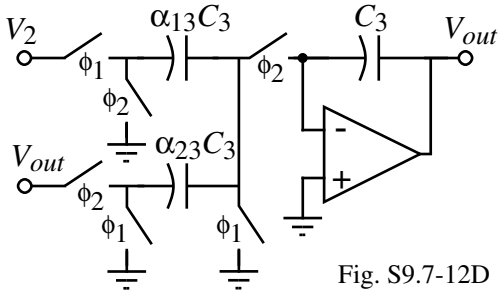


Fig. S9.7-12D

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{13}V_2 - \alpha_{23}V_{out}]$$

Comparing with the third state equation:

$$\frac{\alpha_{13}}{T_n} = \frac{1}{R_{4n}L_{3n}}$$

$$\alpha_{13} = \frac{T_n}{R_{4n}L_{3n}} = \frac{\Omega_n}{R_{4n}f_cL_{3n}} = \frac{1\cdot 2000\pi}{1\cdot 10^5}$$

$$\alpha_{13} = \pi/50 = \underline{\underline{0.0628}} = \alpha_{23}$$

Connect the above three circuits together to get the resulting filter.

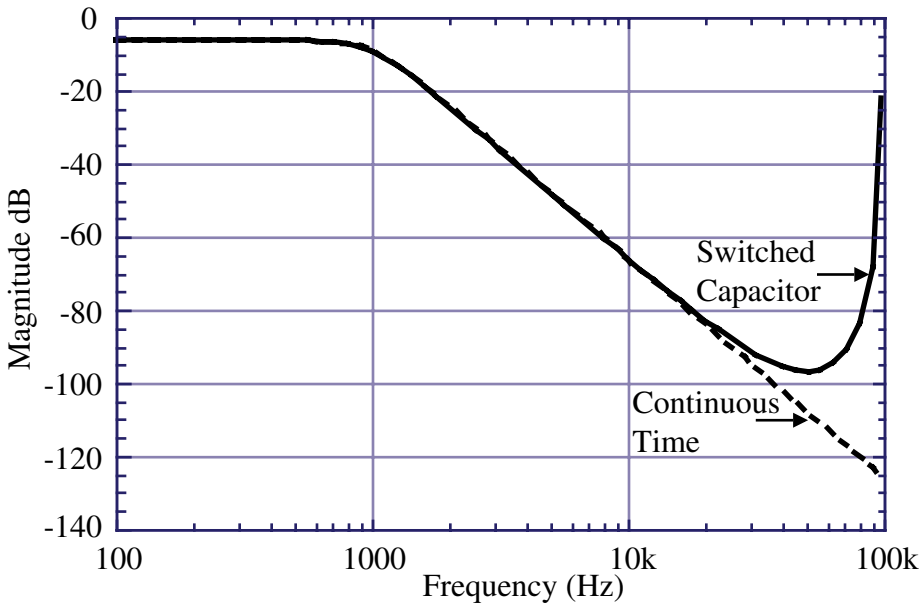
The $C_{max}/C_{min} = 1/\alpha_{12} = \underline{\underline{31.83}}$. The units of capacitances normalized to each integrating capacitor is 3 + (1/0.0628) = 18.91 for the first stage, 2 + (1/0.0314) = 33.83 for the second stage and 2 + (1/0.0628) = 17.91for the third stage. The total units of capacitance for this filter is $\underline{\underline{70.66 \text{ units}}}$.

The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-12
*** Node 13 and 14 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 9 10 3 4 PC1
XPC31 5 6 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** V2 STAGE ***
XNC12 5 6 7 8 NC2
XPC22 13 14 7 8 PC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** VOUT STAGE ***
XNC13 9 10 11 12 NC1
XPC23 13 14 11 12 PC1
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** RLC LADDER NETWORK ***
R1 1 21 50
L1 21 22 7.9577E-3
C2 22 0 6.3662E-6
L3 22 23 7.9577E-3
R2 23 0 50
*************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 15.9155
```

Problem 9.7-12 – Continued

```
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.062832
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.062832
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.062832
RNC2 4 0 15.9155
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 31.831
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.031416
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.031416
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.031416
RNC2 4 0 31.831
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 15.9155
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 31.831
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 100 10 199K
.PRINT AC VDB(13) VDB(14) VDB(23) VP(13) VP(14) VP(23)
.END
```



Problem 9.7-13

Design a switched capacitor realization of the low-pass prototype filter shown in Fig. 9.7-13 assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

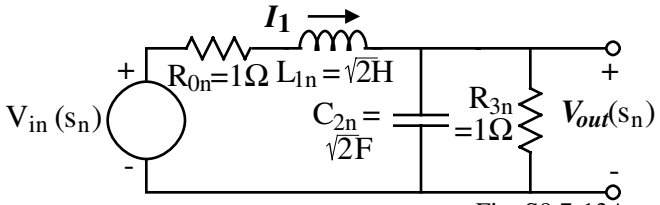


Fig. S9.7-13A

Solution

The state equations are:

$$V_{in} = I_1 R_{on} + sL_{1n} I_1 + V_{out} \quad \rightarrow \quad \boxed{V_1' = \frac{R}{sL_{1n}}\left(V_{in} - \frac{V_1' R_{on}}{R} - V_{out}\right)}$$

$$I_1 - \frac{V_{out}}{R_{3n}} = sC_{2n} V_{out} \quad \rightarrow \quad \boxed{V_{out} = \frac{1}{sRC_{2n}}\left(V_1' - \frac{R}{R_{3n}} V_{out}\right)}$$

The normalized realizations for these equations are:

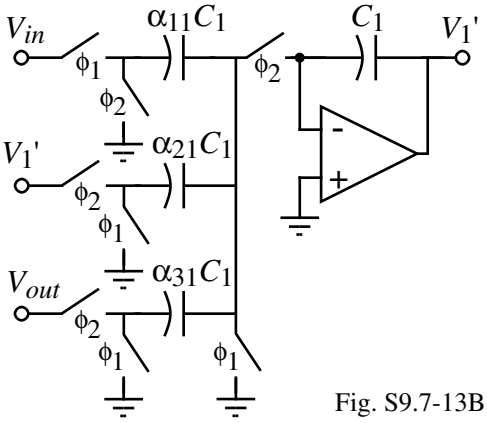


Fig. S9.7-13B

$$V_1' \approx \frac{1}{sT_n}\left[\alpha_{11} V_{in} - \alpha_{21} V_1' - \alpha_{31} V_{out}\right]$$

Comparing with the first state equation:

$$\frac{\alpha_{11}}{T_n} = \frac{R}{L_{1n}} \rightarrow \alpha_{11} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n}{f_c L_{1n}} = \frac{1 \cdot 2000\pi}{10^5 \cdot \sqrt{2}}$$

$$\alpha_{11} = \underline{\underline{0.04443}} = \alpha_{21}$$

$$\frac{\alpha_{31}}{T_n} = \frac{R_{on}}{L_{1n}} \rightarrow \alpha_{31} = \frac{R_{on}\Omega_n}{f_c L_{1n}} = \alpha_{11} = \underline{\underline{0.04443}}$$

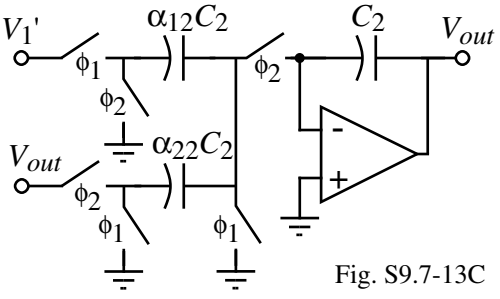


Fig. S9.7-13C

$$V_{out} \approx \frac{1}{sT_n}\left[\alpha_{12} V_1' - \alpha_{22} V_{out}\right]$$

Comparing with the second state equation:

$$\frac{\alpha_{12}}{T_n} = \frac{1}{RC_{2n}} \rightarrow \alpha_{12} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n}{Rf_c C_{2n}} = \frac{1 \cdot 2000\pi}{1 \cdot 10^5 \cdot \sqrt{2}}$$

$$\alpha_{12} = \underline{\underline{0.04443}} = \alpha_{22}$$

Connect the above two circuits together to get the resulting filter.

Problem 9.7-13 – Continued

The $C_{max}/C_{min} = 1/\alpha_{12} = \underline{\underline{22.508}}$. The units of capacitances normalized to each integrating capacitor is 3 + (1/0.04443) = 25.51 for the first stage and 2 + (1/0.0314) = 24.51 for the second stage. The total units of capacitance for this filter is $\underline{\underline{50.158 \text{ units}}}$.

The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-13
*** Node 9 and 10 are Switched Cap outputs
*** Node 22 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 5 6 3 4 PC1
XPC31 9 10 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** VOUT STAGE ***
XNC12 5 6 7 8 NC2
XPC22 9 10 7 8 PC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** RLC LADDER NETWORK ***
R1 1 21 50
L1 21 22 11.254E-3
C2 22 0 4.50158E-6
R2 22 0 50
*************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 22.5079
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.04443
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.04443
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.04443
RNC2 4 0 22.5079
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 22.5079
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.04443
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.04443
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.04443
RNC2 4 0 22.5079
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 22.5079
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 22.5079
```

Problem 9.7-13

```
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 20 10 199K
.PRINT AC VDB(9) VDB(10) VDB(23) VP(9) VP(10) VP(23)
.END
```

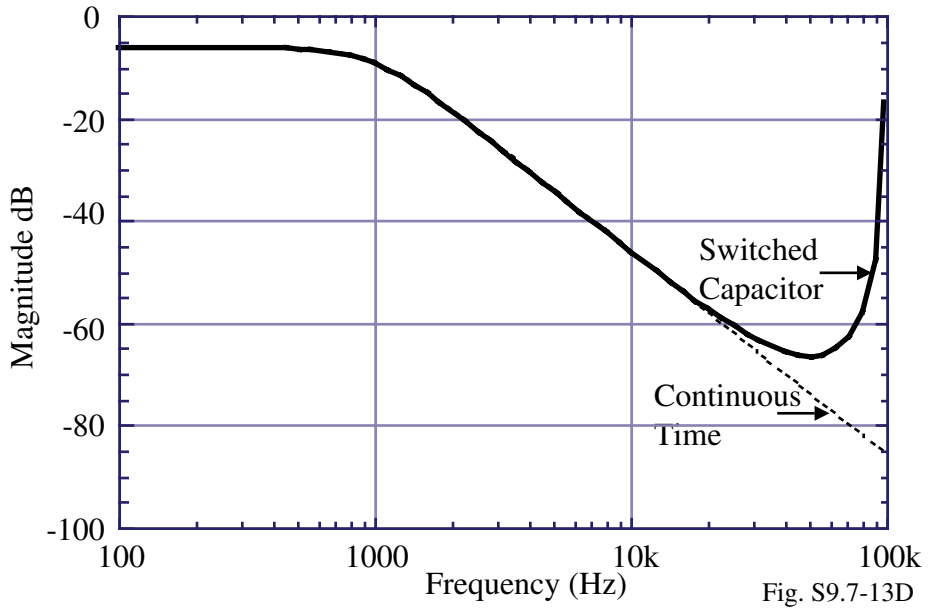


Fig. S9.7-13D

Problem 9.7-14

Design a switched capacitor realization of the low-pass prototype filter shown assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is C_{max}/C_{min}?

Solution

First normalize T by $\Omega_n = 2000\pi$ to get $T_n = \Omega_n T = 2000\pi/100{,}000 = 0.06283$
The state equations are:

$$V_{in} = (I_2 + sC_{1n}V_1)R_{0n} + V_1 \quad \rightarrow \qquad V_1 = \frac{1}{sR_{0n}C_{1n}}\left[V_{in} - V_1 - \frac{R_{0n}}{R}V_2'\right]$$

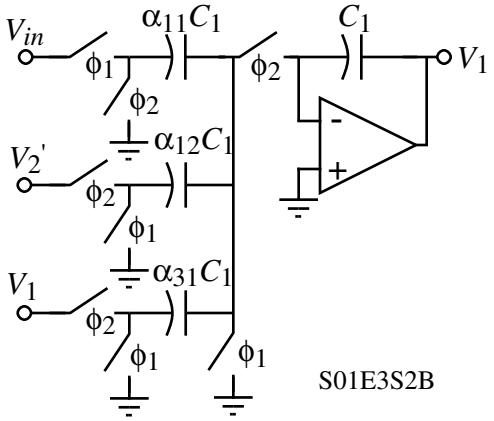
and

$$V_1 = I_2 sL_{2n} + I_2 R_{3n} \quad \rightarrow V_1 = \frac{sL_{2n}}{R} + \frac{R_{3n}}{R}V_2' \quad \rightarrow V_2' = \frac{R}{sL_{2n}}\left[V_1 - \frac{R_{3n}}{R}V_2'\right]$$

Since $V_2' = V_{out}$, we can write

$$V_{out} = \frac{R}{sL_{2n}}\left[V_1 - \frac{R_{3n}}{R}V_{out}\right]$$

Realization of the first state equation:



S01E3S2B

$$V_1(z) = \left(\frac{1}{z_n - 1}\right)[\alpha_{11}V_{in} - \alpha_{21}V_2' - \alpha_{31}V_1]$$

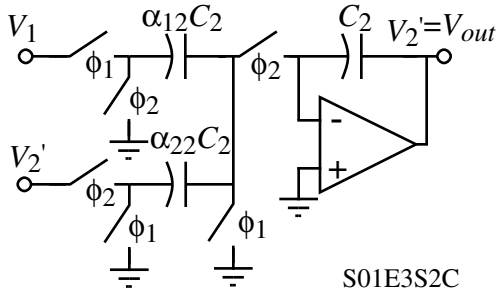
Let $z_n \approx 1 + s_n T_n$ to get

$$V_1(s) = \frac{1}{s_n T_n}[\alpha_{11}V_{in}(s_n) - \alpha_{21}V_2'(s_n) - \alpha_{31}V_1(s_n)]$$

$$\therefore \ \alpha_{11} = \frac{RT_n}{R_{0n}C_{1n}} = \frac{\Omega_n}{f_c C_{1n}} = \frac{2000\pi}{\sqrt{2}\ 10^5} = 0.0444$$

Since, $R = R_{0n}$, then $\underline{\underline{\alpha_{21} = \alpha_{31} = \alpha_{11} = 0.4444}}$

Realization of the second state equation:



S01E3S2C

$$V_{out}(z) = \left(\frac{1}{z_n - 1}\right)[\alpha_{12}V_1 - \alpha_{22}V_2']$$

Let $z_n \approx 1 + s_n T_n$ to get

$$V_{out}(s) = \frac{1}{s_n T_n}[\alpha_{12}V_1(s_n) - \alpha_{22}V_2'(s_n)]$$

$$\therefore \ \alpha_{12} = \frac{T_n}{L_{2n}} = \frac{\Omega_n}{f_c L_{2n}} = \frac{2000\pi}{\sqrt{2}\ 10^5} = 0.0444$$

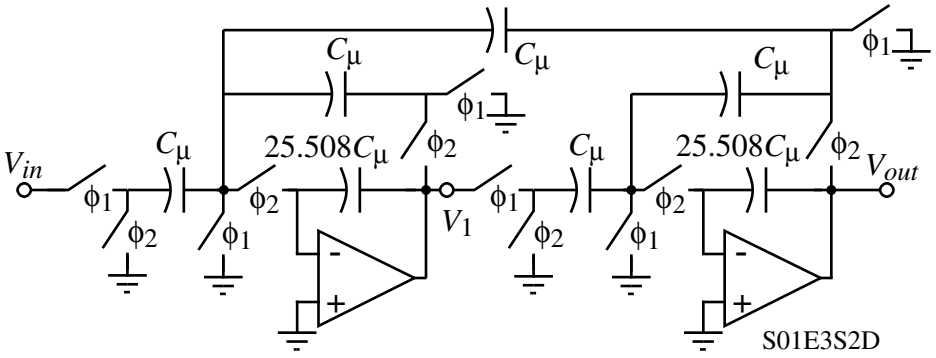
$$\underline{\underline{\alpha_{12} = \alpha_{22} = 0.4444}}$$

Problem 9.7-14 – Continued

$$\frac{C_{max}}{C_{min}} = \frac{1}{0.0444} = \underline{\underline{22.508}}$$

$$\Sigma C = [(22.508+3) + (22.508+2)]C_\mu = \underline{\underline{50.0158C_\mu}}$$

Realization:



Problem 9.7-15

Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C. Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}? Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

Solution

The state equations are:

$$V_{in} = sL_{1n}I_1 + V_2 \quad \rightarrow \quad I_1 = \frac{1}{sL_{1n}}(V_{in} - V_2) \quad \rightarrow \quad \boxed{V_1' = \frac{R}{sL_{1n}}(V_{in} - V_2)}$$

$$V_2 = \frac{1}{sC_{2n}}(I_1 - I_3) \quad \rightarrow \quad V_2 = \frac{1}{sRC_{2n}}(V_1' - V_3') \quad \rightarrow$$

$$\boxed{V_2 = \frac{1}{sRC_{2n}}\left(V_1' - \frac{R}{R_{4n}}V_2\right)}$$

$$I_3 = \frac{1}{sL_{3n}}(V_2 - V_{out}) \quad \rightarrow \quad V_{out} = I_3R_{4n} \quad \rightarrow \quad \boxed{V_{out} = \frac{R_{4n}}{sL_{3n}}(V_2 - V_{out})}$$

The normalized realizations for these equations are:

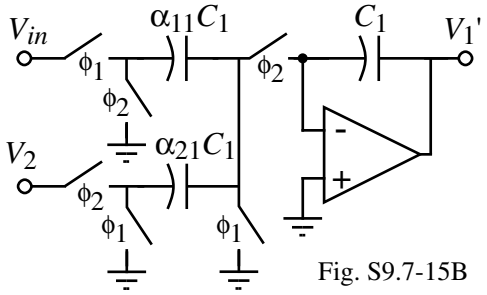


Fig. S9.7-15B

$$V_1' \approx \frac{1}{sT_n}[\alpha_{11}V_{in} - \alpha_{21}V_2]$$

Comparing with the first state equation:

$$\frac{\alpha_{11}}{T_n} = \frac{R}{L_{1n}} \rightarrow \alpha_{11} = \frac{RT_n}{L_{1n}} = \frac{R\Omega_n}{f_cL_{1n}} = \frac{1\cdot 2000\pi}{10^5\cdot 0.5}$$

$$\alpha_{11} = \underline{\underline{0.125664}} = \alpha_{21}$$

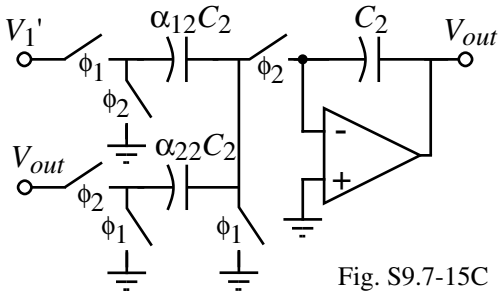


Fig. S9.7-15C

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{12}V_1' - \alpha_{22}V_{out}]$$

Comparing with the second state equation:

$$\frac{\alpha_{12}}{T_n} = \frac{1}{RC_{2n}} \rightarrow \alpha_{12} = \frac{T_n}{RC_{2n}} = \frac{\Omega_n}{Rf_cC_{2n}} = \frac{2000\pi}{10^5\cdot(4/3)}$$

$$\alpha_{12} = \underline{\underline{0.047124}} = \alpha_{22}$$

Problem 9.7-15 – Continued

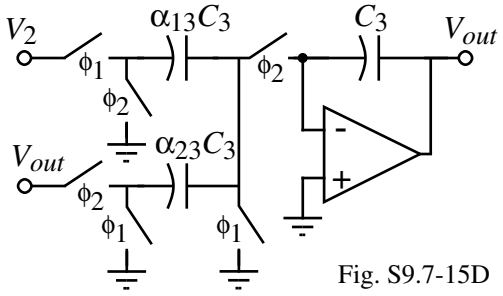


Fig. S9.7-15D

$$V_{out} \approx \frac{1}{sT_n}[\alpha_{13}V_2 - \alpha_{23}V_{out}]$$

Comparing with the third state equation:

$$\frac{\alpha_{13}}{T_n} = \frac{1}{R_{4n}L_{3n}}$$

$$\alpha_{13} = \frac{T_n}{R_{4n}L_{3n}} = \frac{\Omega_n}{R_{4n}f_cL_{3n}} = \frac{2000\pi}{10^5(3/2)}$$

$$\alpha_{13} = \underline{\underline{0.041888}} = \alpha_{23}$$

Connect the above three circuits together to get the resulting filter.

The $C_{max}/C_{min} = 1/\alpha_{13} = \underline{\underline{23.87}}$. The units of capacitances normalized to each integrating capacitor is 2 + (1/0.126) = 9.936 for the first stage, 2 + (1/0.0471) = 23.231 for the second stage and 2 + (1/0.0419) = 25.8671for the third stage. The total units of capacitance for this filter is $\underline{\underline{59.03 \text{ units}}}$.

The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-15
*** Node 13 and 14 are Switched Cap outputs
*** Node 22 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 9 10 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** V2 STAGE ***
XNC12 5 6 7 8 NC2
XPC22 13 14 7 8 PC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** VOUT STAGE ***
XNC13 9 10 11 12 NC3
XPC23 17 18 11 12 PC3
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** RLC LADDER NETWORK ***
L1 1 21 3.9789E-3
C2 21 0 4.2441E-6
L3 21 22 11.9366E-3
R4 22 0 50
*************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 7.957729
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.125664
```

Problem 9.7-15 – Continued

```
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.125664
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.125664
RNC2 4 0 7.957729
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 21.2206
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.047124
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.047124
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.047124
RNC2 4 0 21.2206
.ENDS NC2
.SUBCKT NC3 1 2 3 4
RNC1 1 0 23.8732
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.041888
XNC2 1 4 14 DELAY
GNC2 4 1 14 0.041888
XNC3 4 0 40 DELAY
GNC3 4 0 40 0.041888
RNC2 4 0 23.8732
.ENDS NC3
.SUBCKT PC1 1 2 3 4
RPC1 2 4 7.957729
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 21.2206
.ENDS PC2
.SUBCKT PC3 1 2 3 4
RPC1 2 4 23.8732
.ENDS PC3
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 20 10 200K
.PRINT AC VDB(13) VDB(14) VDB(22)
+VP(13) VP(14) VP(22)
.END
```

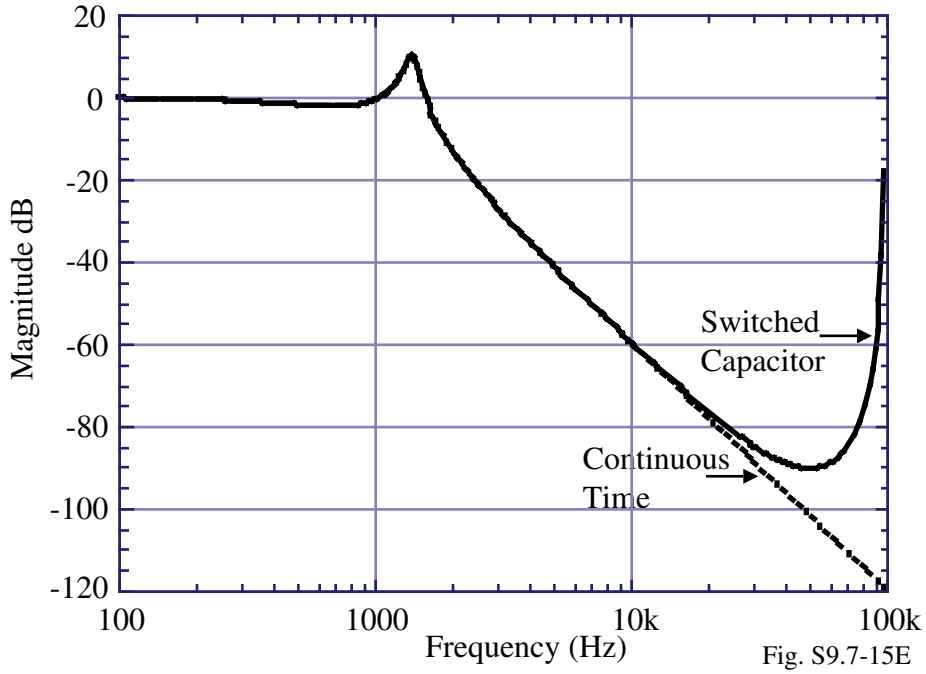
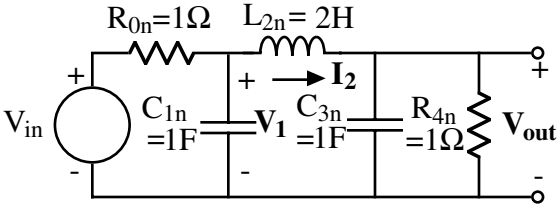


Fig. S9.7-15E

Problem 9.7-16

Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 100 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C (the capacitor connected from op amp output to inverting input). Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}?



Solution

Normalize $T = 1/f_c$ by $\Omega_n = 2000\pi$ to get $T_n = \Omega_n T$.

State Equations:

1.) $\dfrac{V_{in} - V_1}{R_{0n}} = sC_{1n}V_1 + I_2 \Rightarrow V_1 = \dfrac{1}{sC_{1n}}\left(\dfrac{V_{in}}{R_{0n}} - \dfrac{V_1}{R_{0n}} - I_2\right) = \dfrac{1}{sC_{1n}R_{0n}}\left(V_{in} - V_1 - \dfrac{R_{0n}V_2'}{R}\right)$

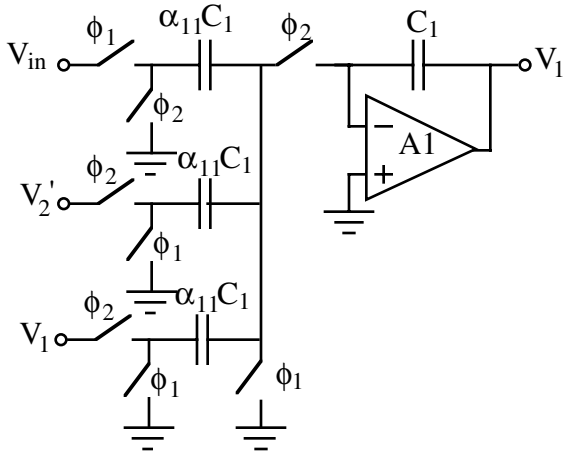
or $\boxed{V_1 = \dfrac{1}{sC_{1n}R_{0n}}\left(V_{in} - V_1 - \dfrac{R_{0n}V_2'}{R}\right)}$ where $V_2' = RI_2$

2.) $I_2 = \dfrac{1}{sL_{2n}}(V_1 - V_{out}) \Rightarrow \boxed{V_2' = \dfrac{R}{sL_{2n}}(V_1 - V_{out})}$

3.) $I_2 = sC_{3n}V_{out} + \dfrac{V_{out}}{R_{4n}} \Rightarrow V_{out} = \dfrac{1}{sC_{3n}}\left(I_2 - \dfrac{V_{out}}{R_{4n}}\right) \Rightarrow \boxed{V_{out} = \dfrac{1}{sC_{3n}R}\left(V_2' - \dfrac{RV_{out}}{R_{4n}}\right)}$

Realizations (Assume $R = R_{0n} = R_{4n}$):

1.)



$V_1 = \dfrac{1}{z_n - 1}\left[\alpha_{11}V_{in} - \alpha_{11}z_nV_2' - \alpha_{11}z_nV_1\right]$

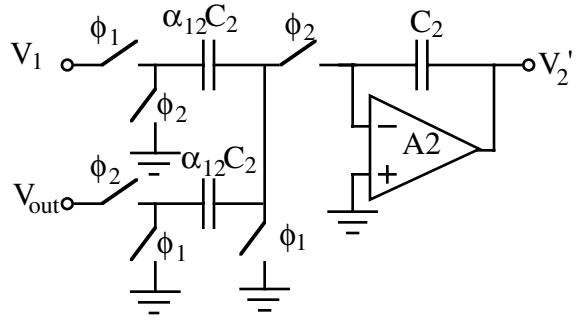
Assume $sT_n << 1$ and let $z_n \approx 1 + sT_n$ to get

$V_1(s) \approx \dfrac{\alpha_{11}}{sT_n}(V_{in} - V_2' - V_1)$

$\therefore \alpha_{11} = \dfrac{T_n}{C_{1n}R_{0n}} = \dfrac{2000\pi}{10^5 \cdot 1} = 0.0628$

Problem 9.7-16 – Continued

2.)



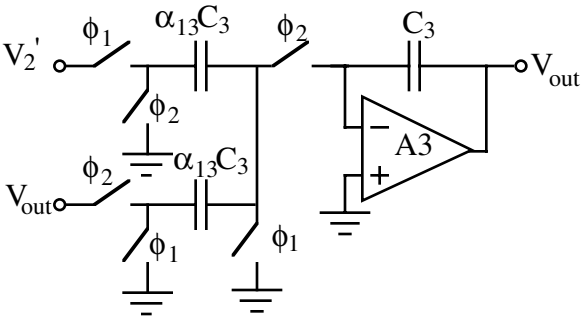
$$V_2' = \frac{1}{z_n - 1}\left[\alpha_{12}V_1 - \alpha_{12}z_n V_{out}\right]$$

Assume $sT_n << 1$ and let $z_n \approx 1 + sT_n$ to get

$$V_1(s) \approx \frac{\alpha_{12}}{sT_n}(V_1 - V_{out})$$

$$\therefore\ \alpha_{12} = \frac{RT_n}{L_{2n}} = \frac{2000\pi}{10^5 \cdot 2} = 0.0314$$

3.)



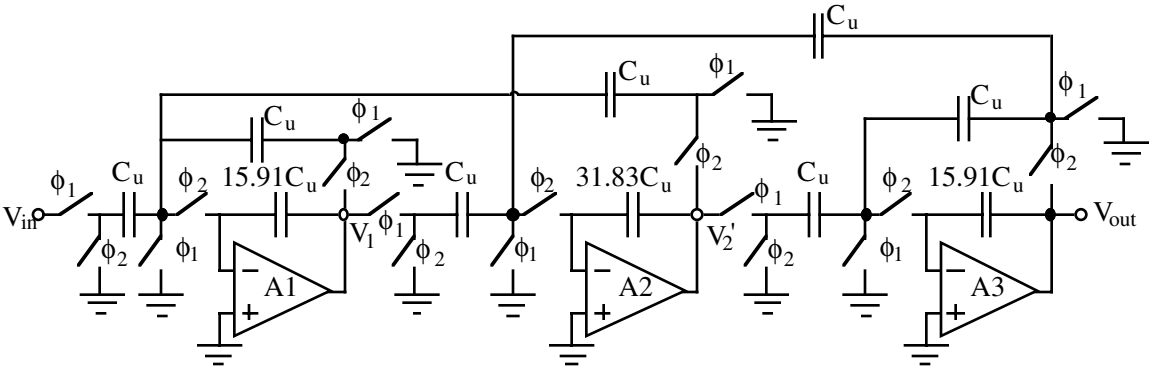
$$V_{out} = \frac{1}{z_n - 1}\left[\alpha_{13}V_2' - \alpha_{13}z_n V_{out}\right]$$

Assume $sT_n << 1$ and let $z_n \approx 1 + sT_n$ to get

$$V_{out}(s) \approx \frac{\alpha_{13}}{sT_n}(V_2' - V_{out})$$

$$\therefore\ \alpha_{12} = \frac{T_n}{RC_{3n}} = \frac{2000\pi}{10^5 \cdot 1} = 0.0628$$

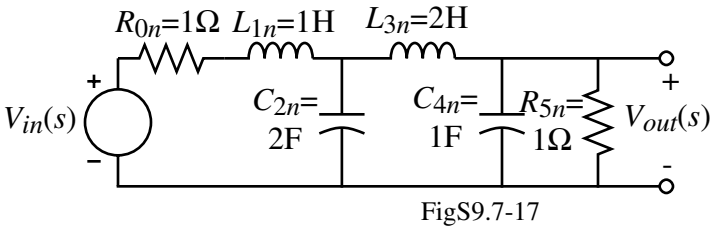
Final Realization is given as:



The total capacitance is $70.65C_u$ where C_u is a unit capacitance. The largest C_{max}/C_{min} ratio is 31.83.

Problem 9.7-17

Design a switched capacitor realization of the low-pass prototype filter shown below assuming a clock frequency of 200 kHz. The passband frequency is 1000Hz. Express each capacitor in terms of the integrating capacitor C (the capacitor connected from op amp output to inverting input). Be sure to show the phasing of the switches using ϕ_1 and ϕ_2 notation. What is the total capacitance in terms of a unit capacitance, C_u? What is largest C_{max}/C_{min}?



FigS9.7-17

Solution

First we must normalize the clock period, T, by $\Omega_n = 2000\pi$ to get $T_n = \Omega_n T = \Omega_n / f_c$.

The state equations for the bold variables above are:

1.) $V_{in} = R_{0n} I_1 + sL_1 I_1 + V_2 = \frac{R_{0n}}{R} V_1' + \frac{sL_1}{R} V_1' + V_2 \rightarrow V_1' = \frac{R}{sL_{1n}} \left(V_{in} - \frac{R_{0n}}{R} V_1' - V_2 \right)$

2.) $V_2 = \frac{1}{sRC_{2n}} (V_1' - V_3')$

3.) $V_3' = \frac{R}{sL_{3n}} (V_2 - V_{out})$

4.) $I_3 = sC_{4n} V_{out} + \frac{V_{out}}{R_{5n}} \rightarrow V_{out} = \frac{1}{sRC_{4n}} \left(V_3' - \frac{R}{R_{5n}} V_{out} \right)$

Realizing each of these four state equations is done as follows:

1.) $V_1'(z_n) = \frac{1}{z_n - 1} [\alpha_{11} V_{in} - \alpha_{11} z_n V_2 - \alpha_{11} z_n V_1']$

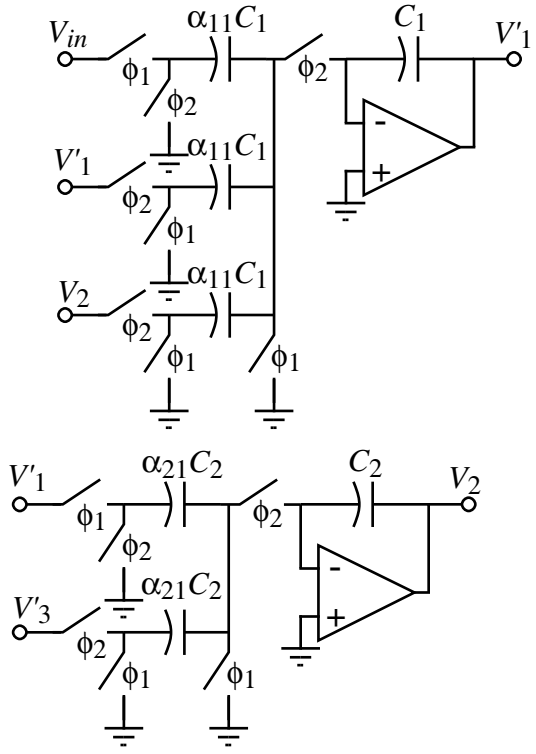
$$V_1'(s) \approx \frac{\alpha_{11}}{sT_n} [V_{in} - V_2 - V_1']$$

$$\therefore \ \alpha_{11} = \frac{T_n R}{L_{1n}} = \frac{2000\pi}{10^5 \cdot 1} = 0.0314$$

2.) $V_2(z_n) = \frac{1}{z_n - 1} [\alpha_{21} V_1' - \alpha_{21} z_n V_3']$

$$V_2(s) \approx \frac{\alpha_{21}}{sT_n} [V_1' - V_3']$$

$$\therefore \ \alpha_{21} = \frac{T_n}{RC_{2n}} = \frac{2000\pi}{10^5 \cdot 2} = 0.0159$$

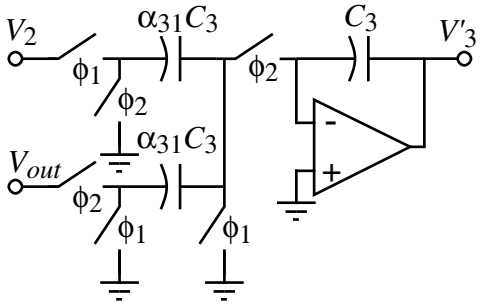


Problem 9.7-17 - Continued

3.) $V_3'(z_n) = \frac{1}{z_n - 1}[\alpha_{31}V_2 - \alpha_{31}z_n V_{out}]$

$$V_3'(s) \approx \frac{\alpha_{31}}{sT_n}[V_2 - V_{out}]$$

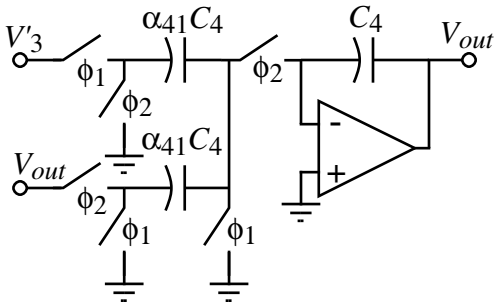
$$\therefore \ \alpha_{31} = \frac{T_n R}{L_{3n}} = \frac{2000\pi}{10^5 \cdot 2} = 0.0159$$



4.) $V_{out}(z_n) = \frac{1}{z_n - 1}[\alpha_{41}V_3' - \alpha_{41}z_n V_{out}]$

$$V_{out}(s) \approx \frac{\alpha_{41}}{sT_n}[V_3' - V_{out}]$$

$$\therefore \ \alpha_{41} = \frac{T_n}{RC_{4n}} = \frac{2000\pi}{10^5 \cdot 1} = 0.0314$$



The actual filter realization is obtained by connecting the above four circuits as indicated by their terminal voltages.

Total capacitance:

For each stage, make the smallest capacitor equal to C_u and sum capacitors.

Stage 1: $3C_u + (C_u/0.0314) = 31.8C_u + 3C_u = 34.8C_u$
Stage 2: $2C_u + (C_u/0.0159) = 63.7C_u + 2C_u = 65.7C_u$
Stage 3: $2C_u + (C_u/0.0159) = 63.7C_u + 2C_u = 65.7C_u$
Stage 4: $2C_u + (C_u/0.0314) = 31.8C_u + 2C_u = 33.8C_u$
Total capacitance = $200C_u$

$$\frac{C_{max}}{C_{min}} = 63.7$$

SPICE File:

```
*** HW9 PROBLEM3 (Problem 9.7-17) ***
*** Node 17 and 18 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1' STAGE ***
XNC11 1 2 3 4 NC1
XPC21 9 10 3 4 PC1
XPC31 5 6 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP

*** V2 STAGE ***
XNC12 5 6 7 8 NC2
XPC22 13 14 7 8 PC2
```

Problem 9.7-17 – Continued

```
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** V3' STAGE ***
XNC13 9 10 11 12 NC2
XPC23 17 18 11 12 PC2
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** VOUT STAGE ***
XNC14 13 14 15 16 NC1
XPC24 17 18 15 16 PC1
XUSCP4 15 16 17 18 USCP
XAMP4 15 16 17 18 AMP
*** RLC LADDER NETWORK ***
R1 1 21 50
L1 21 22 7.9577E-3
C2 22 0 6.3662E-6
L3 22 23 15.9155E-3
C4 23 0 3.1831E-6
R2 23 0 50
*************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=2.5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 31.8269
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.03142
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.03142
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.03142
RNC2 4 0 31.8269
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 63.6537
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.01571
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.01571
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.01571
RNC2 4 0 63.6537
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 31.8269
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 63.6537
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 1000 10 199K
.PROBE
.END
```

Problem 9.7-18

Use the low-pass, normalized prototype filter of Fig. P9.7-14 to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 500Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

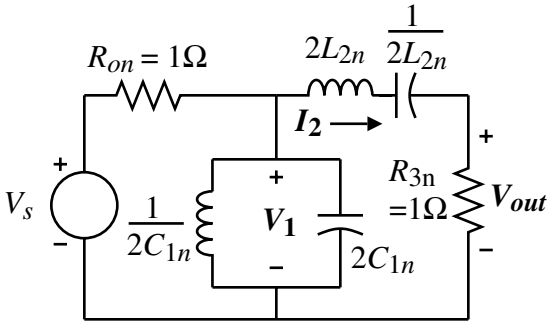
Solution

1.) Normalize by $s = \left(\frac{\omega_r}{BW}\right)p = \frac{1000}{500}p = 2p$

2.) Transform the normalized circuit to bandpass using the transformation,

$$s = p + \frac{1}{p}$$

The resulting circuit is shown.



3.) The state equations for this bandpass circuit can be written as follows.

$$V_1 = \frac{\frac{s}{2RC_{1n}}}{s^2+1}\left[\frac{R}{R_{on}}(V_{in}-V_1)-V_2'\right]$$

where $V_2' = I_2 \cdot R$ and $R = 1$.

$$V_{out} = \frac{R_{3n}}{R}\ V_2' = \frac{R_{3n}}{R}\left(\frac{\frac{sR}{2L_{2n}}}{s^2+1}\right)(V_1-V_{out}) = \left(\frac{\frac{sR_{3n}}{2L_{2n}}}{s^2+1}\right)(V_1-V_{out})$$

4.) The SC realization of each second-order block is given as,

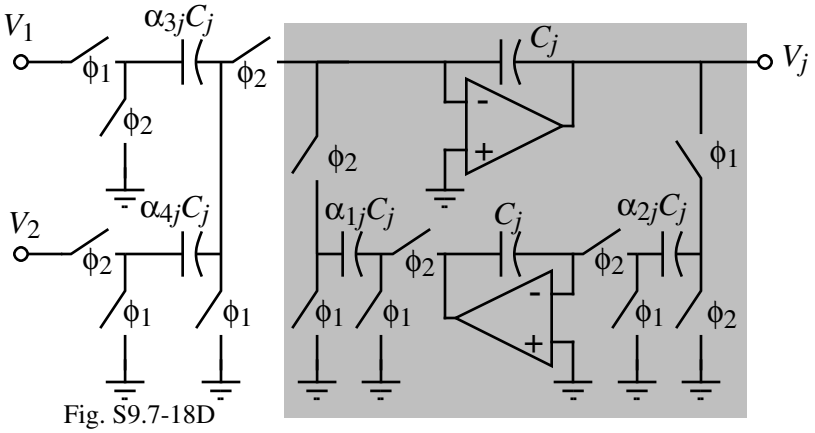


Fig. S9.7-18D

Problem 9.7-18 – Continued

If $f_{clock}>>f_r$, then $V_j(s)$ of the above realization can be written as,

$$V_j(s) \approx \left(\frac{s}{s^2 + \frac{\alpha_{1j}\alpha_{2j}}{T_n^2}} \right) \left[\frac{\alpha_{3j}}{T_n} V_1 - \frac{\alpha_{4j}}{T_n} V_2 \right] \qquad \text{where } T_n = \Omega_n T = \omega_r T$$

5.) Comparing the state equations with the above transfer function gives,

$j = 1$ or V_1: $\alpha_{11}\alpha_{21} = T_n^2 \rightarrow \alpha_{11} = \alpha_{21} = T_n = \omega_r T = \frac{\omega_r}{f_{clock}} = \frac{2\pi \text{x} 10^3}{10^5} = \underline{\underline{0.02\pi}}$

$$\alpha_{31} = \alpha_{41} = \alpha_{51} = \frac{T_n}{R_{on} 2 C_{1n}} = \frac{\omega_r T}{2\sqrt{2}} = \frac{2\pi \text{x} 10^3}{2\sqrt{2} \text{x} 10^5} = \underline{\underline{0.0071\pi}}$$

$j = 2$ or V_{out}: $\alpha_{12}\alpha_{22} = T_n^2 \rightarrow \alpha_{12} = \alpha_{22} = T_n = \omega_r T = \frac{\omega_r}{f_{clock}} = \frac{2\pi \text{x} 10^3}{10^5} = \underline{\underline{0.02\pi}}$

$$\alpha_{32} = \alpha_{42} = \frac{T_n}{R_{on} 2 L_{2n}} = \frac{\omega_r T}{2\sqrt{2}} = \frac{2\pi \text{x} 10^3}{2\sqrt{2} \text{x} 10^5} = \underline{\underline{0.0071\pi}}$$

6.) Filter realization:

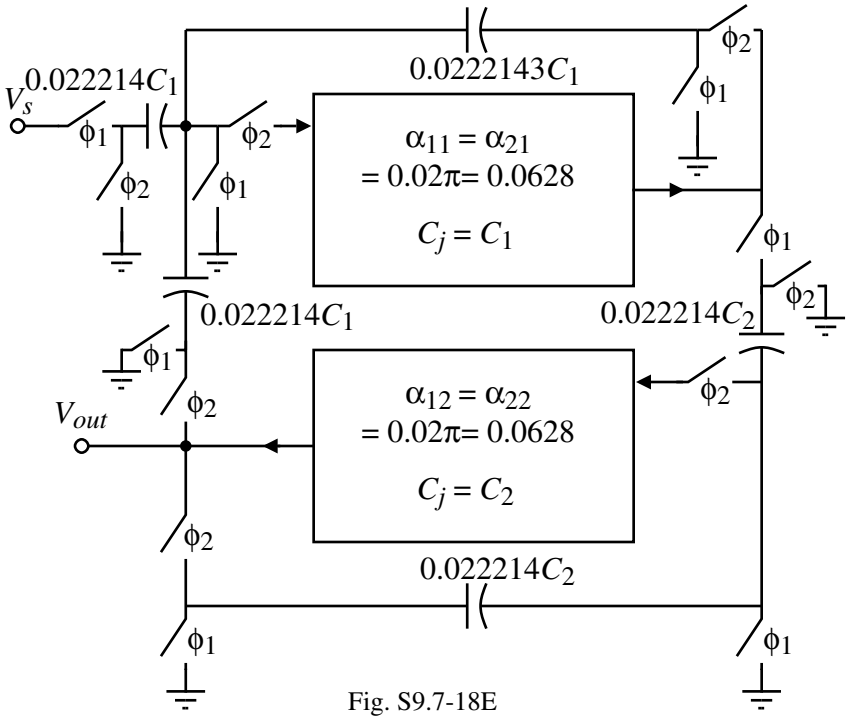


Fig. S9.7-18E

Problem 9.7-18 – Continued

7.) To create the SPICE input file, the above figure needs to be expanded which is done below.

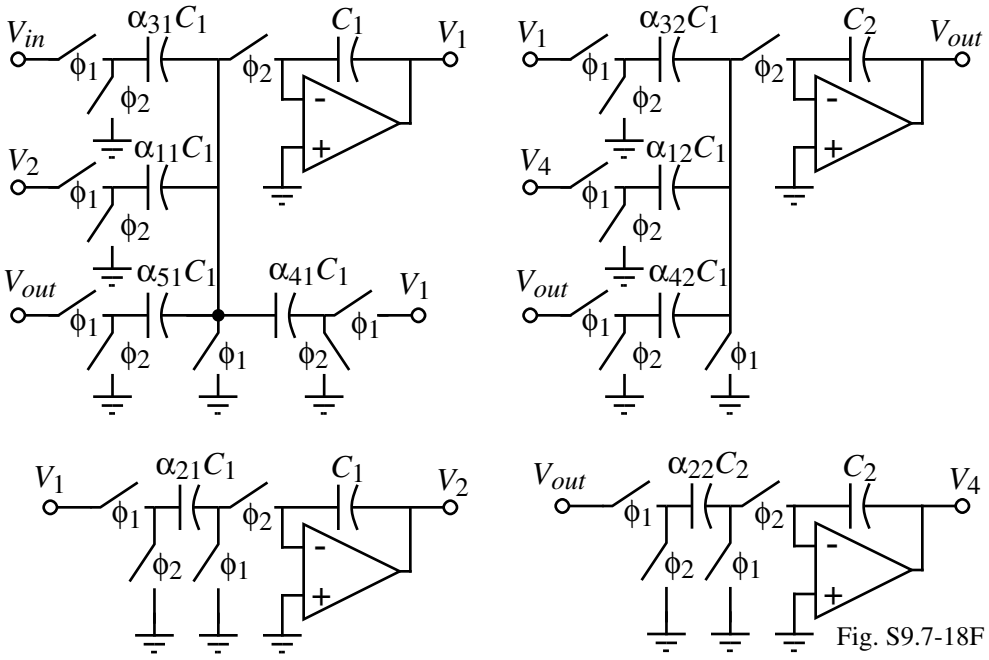


Fig. S9.7-18F

8.) The SPICE simulation file for this filter is shown below.

```
SPICE File for Problem 9.7-18
*** Node 13 and 14 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1 STAGE ***
XPC11 9 10 3 4 PC2
XNC31 1 2 3 4 NC1
XPC41 5 6 3 4 PC1
XPC51 13 14 3 4 PC1
XUSCP1 3 4 5 6 USCP
XAMP1 3 4 5 6 AMP
*** V2 STAGE ***
XNC21 5 6 7 8 NC2
XUSCP2 7 8 9 10 USCP
XAMP2 7 8 9 10 AMP
*** VOUT STAGE ***
XPC12 17 18 11 12 PC2
XNC32 5 6 11 12 NC1
XPC42 13 14 11 12 PC1
XUSCP3 11 12 13 14 USCP
XAMP3 11 12 13 14 AMP
*** V4 STAGE ***
XNC22 13 14 15 16 NC2
XUSCP4 15 16 17 18 USCP
XAMP4 15 16 17 18 AMP
*** RLC LADDER NETWORK ***
R0 1 21 50
C1 21 0 9.0032E-6
L1 21 0 2.8135E-3
```

Problem 9.7-18 – Continued

```
L2 21 22 22.5079E-3
C2 22 23 1.125395E-6
R3 23 0 50
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC1 1 2 3 4
RNC1 1 0 45.015816
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.022214
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.022214
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.022214
RNC2 4 0 45.015816
.ENDS NC1
.SUBCKT NC2 1 2 3 4
RNC1 1 0 15.91549
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.062832
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.062832
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.062832
RNC2 4 0 15.91549
.ENDS NC2
.SUBCKT PC1 1 2 3 4
RPC1 2 4 45.015816
.ENDS PC1
.SUBCKT PC2 1 2 3 4
RPC1 2 4 15.91549
.ENDS PC2
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
*** ANALYSIS ***
.AC DEC 20 100 100K
.PRINT AC VDB(17) VDB(18) VDB(23) VP(17) VP(17) VP(23)
.END
```

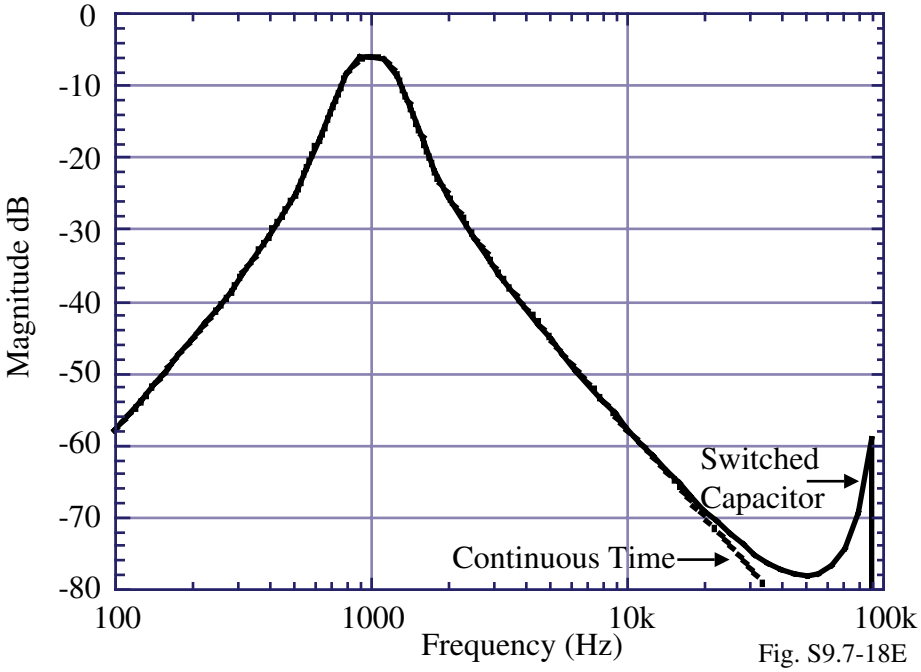


Fig. S9.7-18E

Problem 9.7-19

Use the low-pass, normalized prototype filter of Fig. P9.7-13 to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 500Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

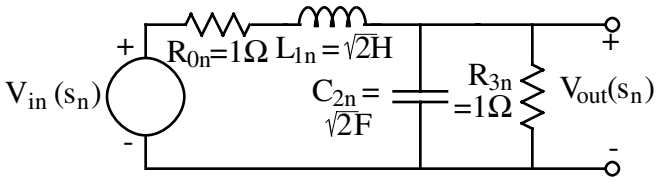


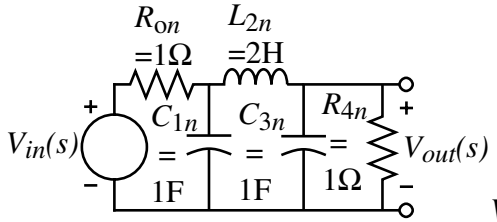
Figure P9.7-13

Solution

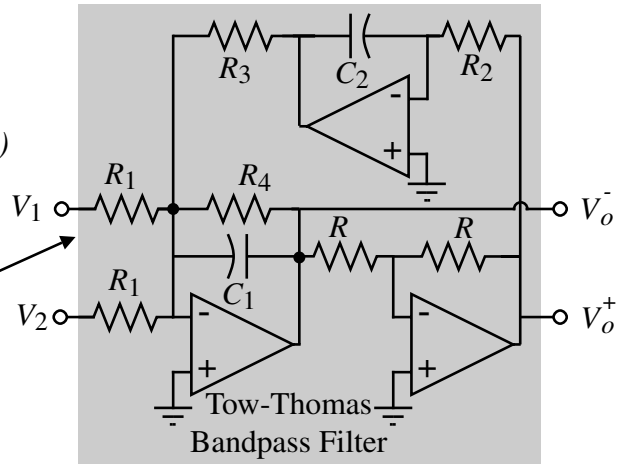
TBD

Problem 9.7-20

Use the low-pass, normalized prototype filter shown to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 100Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

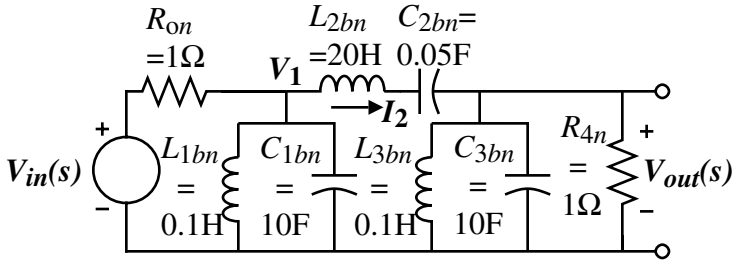


$$-\frac{V_o^-}{V_1}=\frac{V_o^+}{V_1}=\frac{\left(\frac{R_4}{R_1}\right)\frac{s}{R_4C_1}}{s^2+\frac{s}{R_4C_1}+\frac{1}{R_2R_3C_1C_2}}$$



Solution

The bandpass normalized filter is shown using the values of f_r = 1000 Hz and BW = 100 Hz to scale the elements by 10. The state variables and the input voltage are shown in bold.



The state equations are:

1.)

$$\frac{V_{in}-V_1}{R_{0n}}=I_2+(sC_{1bn}+\frac{1}{sL_{1bn}})\,V_1 \;\rightarrow\; \frac{V_{in}}{R_{0n}}-\frac{V_2'}{R}=\left(\frac{1}{R_{0n}}+sC_{1bn}+\frac{1}{sL_{1bn}}\right)V_1$$

or

$$V_1=\frac{\frac{s}{C_{1bn}R}}{s^2+\frac{s}{R_{0n}C_{1bn}}+\frac{1}{L_{1bn}C_{1bn}}}\left(V_2'-\frac{V_{in}}{R_{0n}}\right)=\frac{0.1s}{s^2+0.1s+1}(V_2'-V_{in})$$

2.)

$$I_2=\frac{V_2'}{R}=\frac{V_2-V_{out}}{sL_{2bn}+\frac{1}{sC_{2bn}}}=\frac{\frac{s}{L_{2bn}}}{s^2+\frac{1}{L_{2bn}C_{2bn}}}(V_1-V_{out}) \rightarrow V_2'=\frac{0.05s}{s^2+1}(V_1-V_{out})$$

3.)

$$V_{out}=\frac{\frac{V_2'}{R}}{sC_{3bn}+\frac{1}{sL_{3bn}}+\frac{1}{R_{4n}}}=\frac{0.1V_2'}{s^2+0.01s+1}$$

Problem 9.7-20 - Continued

Now we need to design each Tow-Thomas bandpass circuit. If $R_2 = R_3 = 1\Omega$ and $C_1 = C_2 = 1$F of the Tow-Thomas circuit then the transfer function becomes,

$$\frac{V_o^+}{V_1} = \frac{\frac{s}{R_{i1}}}{s^{2^{\circ\circ}} + \frac{s}{R_{i4}} + 1} \quad \text{where } i \text{ corresponds to the } i\text{-th stage}$$

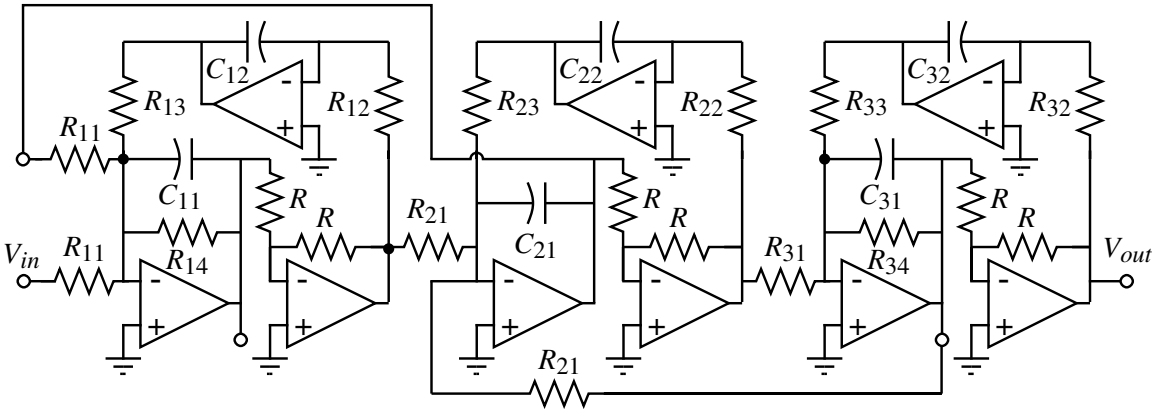
Therefore the design of each stage is:

Stage 1: $R_{11} = 10\Omega$, $R_{14} = 10\Omega$, $R_{12} = R_{13} = 1\Omega$, and $C_{11} = C_{12} = 1$F

Stage 2: $R_{21} = 20\Omega$, $R_{24} = \infty$, $R_{22} = R_{23} = 1\Omega$, and $C_{21} = C_{22} = 1$F

Stage 3: $R_{31} = 10\Omega$, $R_{34} = 10\Omega$, $R_{32} = R_{33} = 1\Omega$, and $C_{31} = C_{32} = 1$F

Next, denormalizing by 2000π and impedance denormalizing by 10^5 gives,



where

$$\boxed{R = R_{11} = R_{14} = 1\text{M}\Omega,\ R_{12} = R_{13} = 100\text{k}\Omega,\ \text{and}\ C_{11} = C_{12} = 1.59\text{nF}}$$

$$\boxed{R = R_{21} = 2\text{M}\Omega,\ R_{24} = \infty,\ R_{22} = R_{23} = 100\text{k}\Omega,\ \text{and}\ C_{21} = C_{22} = 1.59\text{nF}}$$

and

$$\boxed{R = R_{31} = R_{32} = 1\text{M}\Omega,\ R_{32} = R_3 = 100\text{k}\Omega,\ \text{and}\ C_{31} = C_{32} = 1.59\text{nF}}$$

SPICE File:

```
*** HW9 PROBLEM4 (Problem 9.7-20) ***
*** Node 13 and 14 are Switched Cap outputs
*** Node 23 is RLC ladder network output
VIN 1 0 DC 0 AC 1
*** V1 STAGE ***
XNC41 1 2 3 4 NC41
XPC411 9 10 3 4 PC41
XPC412 5 6 3 4 PC41
XLQBQ1 3 4 5 6 LQBIQUAD
```

Problem 9.7-20 – Continued

```
*** V2' STAGE ***
XNC42 5 6 7 8 NC42
XPC421 13 14 7 8 PC42
XLQBQ2 7 8 9 10 LQBIQUAD
*** VOUT STAGE ***
XNC43 9 10 11 12 NC41
XPC431 13 14 11 12 PC41
XLQBQ3 11 12 13 14 LQBIQUAD
*** RLC LADDER NETWORK ***
R1 1 21 50
C11 21 0 3.1831E-5
L11 21 0 7.9577E-4
L21 21 22 0.1592
C21 22 23 1.5915E-7
C31 23 0 3.1831E-5
L31 23 0 7.9577E-4
R2 23 0 50
**************************
*** SUB CIRCUITS ***
.SUBCKT DELAY 1 2 3
ED 4 0 1 2 1
TD 4 0 3 0 ZO=1K TD=5US
RDO 3 0 1K
.ENDS DELAY
.SUBCKT NC5 1 2 3 4
RNC1 1 0 15.916
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.06283
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.06283
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.06283
RNC2 4 0 15.916
.ENDS NC5
.SUBCKT NC41 1 2 3 4
RNC1 1 0 159.1596
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.006283
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.006283
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.006283
RNC2 4 0 159.1596
.ENDS NC41
.SUBCKT NC42 1 2 3 4
RNC1 1 0 318.2686
XNC1 1 0 10 DELAY
GNC1 1 0 10 0 0.003142
XNC2 1 4 14 DELAY
GNC2 4 1 14 0 0.003142
XNC3 4 0 40 DELAY
GNC3 4 0 40 0 0.003142
RNC2 4 0 318.2686
.ENDS NC42
```

Problem 9.7-20 – Continued

```
.SUBCKT PC2 1 2 3 4
RPC1 2 4 15.916
.ENDS PC2
.SUBCKT PC41 1 2 3 4
RPC1 2 4 159.1596
.ENDS PC41
.SUBCKT PC42 1 2 3 4
RPC1 2 4 318.2686
.ENDS PC42
.SUBCKT USCP 1 2 3 4
R1 1 3 1
R2 2 4 1
XUSC1 1 2 12 DELAY
GUSC1 1 2 12 0 1
XUSC2 1 4 14 DELAY
GUSC2 4 1 14 0 1
XUSC3 3 2 32 DELAY
GUSC3 2 3 32 0 1
XUSC4 3 4 34 DELAY
GUSC4 3 4 34 0 1
.ENDS USCP
.SUBCKT AMP 1 2 3 4
EODD 0 3 1 0 1E6
EVEN 0 4 2 0 1E6
.ENDS AMP
.SUBCKT LQBIQUAD 5 6 7 8
XPC2 7 8 1 2 PC2
XUSCP1 1 2 3 4 USCP
XAMP1 1 2 3 4 AMP
XNC5 3 4 5 6 NC5
XUSCP2 5 6 7 8 USCP
XAMP2 5 6 7 8 AMP
.ENDS LQBIQUAD
*** ANALYSIS ***
.AC DEC 1000 10 99K
.PROBE
.END
```

Problem 9.7-21

Use the low-pass, normalized prototype filter shown to develop a switched-capacitor, ladder realization for a bandpass filter which has a center frequency of 1000Hz, a bandwidth of 100Hz, and a clock frequency of 100kHz. Give a schematic diagram showing all values of capacitances in terms of the integrating capacitor and the phasing of all switches. Use strays-insensitive integrators. Use SPICE to plot the frequency response (magnitude and phase) of your design and the ideal continuous time filter.

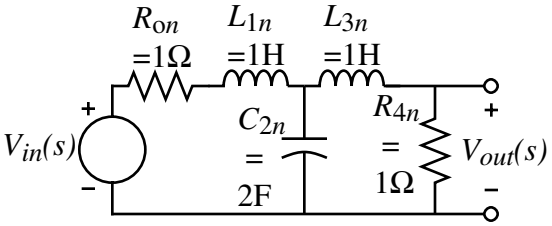


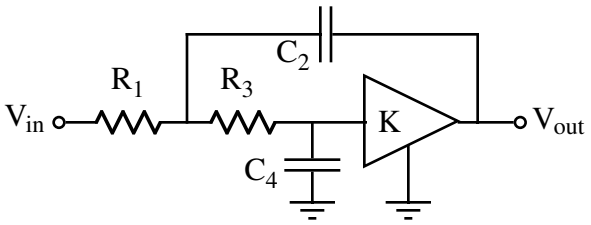
Figure P9.7-21

Solution

TBD

Problem 9.7-22

A second-order, lowpass, Sallen and Key active filter is shown along with the transfer function in terms of the components of the filter.



$$\frac{V_{out}}{V_{in}} = \frac{\frac{K}{R_1R_3C_2C_4}}{s^2+s\left[\frac{1}{R_3C_4} + \frac{1}{R_1C_2} + \frac{1}{R_3C_2} - \frac{K}{R_3C_4}\right] + \frac{1}{R_1R_3C_2C_4}}$$

a.) Define $n = R_3/R_1$ and $m = C_4/C_2$ and let $R_1 = R$ and $C_2 = C$. Develop the design equations for Q and ω_o if K = 1.

b.) Use these equations to design for a second-order, lowpass, Butterworth anti-aliasing filter with a bandpass frequency of 10kHz. Let $R_1 = R = 10k\Omega$ and find the value of C_2, R_3, and C_4.

Solution

a.) The expressions for Q and ω_o are

$$\omega_o = \frac{1}{\sqrt{R_1R_3C_2C_4}} \quad \text{and} \quad \frac{\omega_o}{Q} = \frac{1}{R_3C_4} + \frac{1}{R_1C_2} + \frac{1}{R_3C_2} - \frac{K}{R_3C_4}$$

If K = 1, then $\omega_o = \frac{1}{\sqrt{R_1R_3C_2C_4}}$ and $\frac{1}{Q} = \sqrt{\frac{R_3C_4}{R_1C_2}} + \sqrt{\frac{R_1C_4}{R_3C_2}}$.

Define $n = \frac{R_3}{R_1}$ and $m = \frac{C_4}{C_2}$ and let $R_1 = R$ and $C_2 = C$. Therefore,

$$\omega_o^2 = \frac{1}{mn(R_1C_2)^2} \Rightarrow \boxed{\omega_o = \frac{1}{\sqrt{mn}R_1C_2} = \frac{1}{\sqrt{mn}RC}}$$

and $$\boxed{\frac{1}{Q} = \sqrt{mn} + \sqrt{\frac{m}{n}} = \sqrt{mn}\left(1+\frac{1}{n}\right)}$$

b.) A normalized Butterworth second-order lowpass function is

$$\frac{V_{out}}{V_{in}} = \frac{1}{s^2+\sqrt{2}s+1} \Rightarrow \omega_o = 1 \text{ rad/sec and } Q = 0.707$$

Let $R_1 = R = 1\Omega$ and $C_2 = C = 1F$. $\therefore \sqrt{mn} = 1$ and $\sqrt{2} = 1\cdot\left(1+\frac{1}{n}\right) = 1+\frac{1}{n}$

From the above, $n = \frac{1}{\sqrt{2}-1} = 2.4142$ and $m = \frac{1}{2.4142} = 0.4142$

$\therefore$ $R_3 = 2.4142\Omega$ and $C_4 = 0.4142F$

Denormalizing by $10^4\Omega$ and $20{,}000\pi$ (rads/sec) gives

$$\boxed{R_1 = 10k\Omega,\ R_3 = 24.142k\Omega,\ C_1 = 1.59nF \text{ and } C_4 = 0.659nF}$$

Problem 9.7-23

The circuit shown is to be analyzed to determine its capability to realize a second-order transfer function with complex conjugate poles. Find the transfer function of the circuit and determine and verify the answers to the following questions:

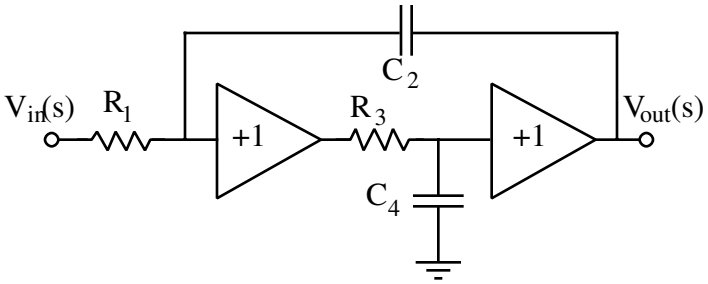


Figure P9.7-23

1.) Is the circuit low-pass, bandpass, high-pass, or other?

2.) Find H_o, ω_o, and Q in terms of R_1, C_2, R_3, and C_4.

3.) What elements would you adjust to independently tune Q and ω_o?

Solution

a.) $$V_{out} = \left(\frac{(1/sC_4)}{R_3+(1/sC_4)}\right)V_1 = \frac{V_1}{sR_3C_4+1}$$

$$V_1 = \left(\frac{R_1}{R_1+(1/sC_2)}\right)V_{out} + \left(\frac{(1/sC_2)}{R_1+(1/sC_2)}\right)V_{in} = \frac{sR_1C_2V_{out}}{sC_2R_1+1} + \frac{V_{in}}{sC_2R_1+1}$$

$\therefore$ $$V_{out} = \left(\frac{1}{sR_3C_4+1}\right)\left(\frac{sR_1C_2V_{out}}{sC_2R_1+1} + \frac{V_{in}}{sC_2R_1+1}\right)$$

$$V_{out}(sR_3C_4+1)(sR_1C_2+1) = sR_1C_2V_{out} + V_{in}$$

$$V_{out}[s^2R_1R_3C_2C_4 + sR_1C_2 + sR_3C_4 - sR_1C_2 + 1] = V_{in}$$

$\therefore$ $$\frac{V_{out}}{V_{in}} = \frac{1}{s^2R_1R_3C_2C_4+sR_3C_4+1} = \frac{\frac{1}{R_1R_3C_2C_4}}{s^2+\frac{s}{R_1C_2} + \frac{1}{R_1R_3C_2C_4}} = \frac{H_o\omega_o^2}{s^2+\left(\frac{\omega_o}{Q}\right)s + \omega_o}$$

$\therefore$ Filter is low-pass.

b.) From the previous results, $H_o = 1$, $\omega_o = \frac{1}{\sqrt{R_1R_3C_2C_4}}$, and $Q = \omega_o R_1C_2 = \sqrt{\frac{R_1C_2}{R_3C_4}}$

c.) To tune ω_o but not Q, adjust the product of R_1R_3 (C_2C_4) keeping the ratio R_1/R_3 (C_2/C_4) constant.

To tune Q but not ω_o, adjust the ratio R_1/R_3 (C_2/C_4) keeping the product of R_1R_3 (C_2C_4) constant.