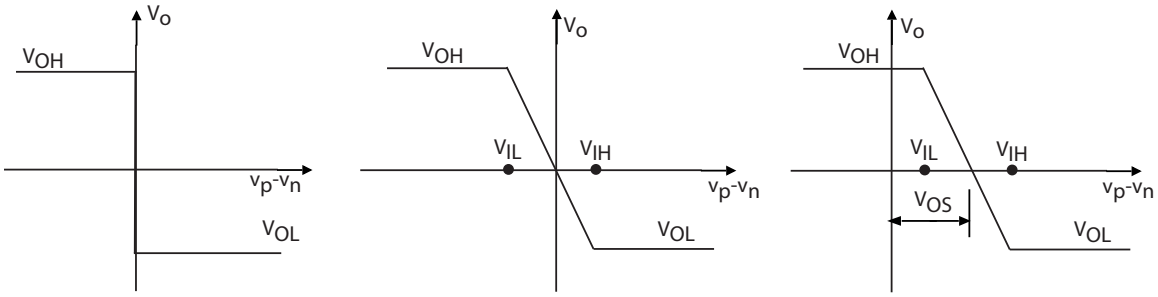
CHAPTER 8 – HOMEWORK SOLUTIONS

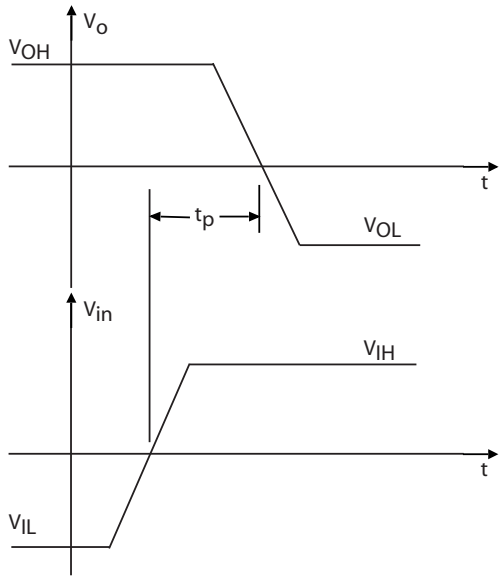
Problem 8.1-01

Give the equivalent figures for Figs. 8.1-2, 8.1-4, 8.1-6 and 8.1-9 for an inverting comparator.

Solution

The figures for the inverting comparator are shown below.





Problem 8.1-02

Use the macromodel techniques of Sec. 6.6 to model a comparator having a dc gain of 10,000 V/V, and offset voltage of 10mV, V_{OH} = 1V, V_{OL} = 0V, a dominant pole at -1000 radians/sec. and a slew rate of 1V/μs. Verify your macromodel by using it to simulate Ex. 8.1-1.

Solution

TBD

Problem 8.1-03

Draw the first-order time response of an inverting comparator with a 20 μs propagation delay. The input is described by the following equation

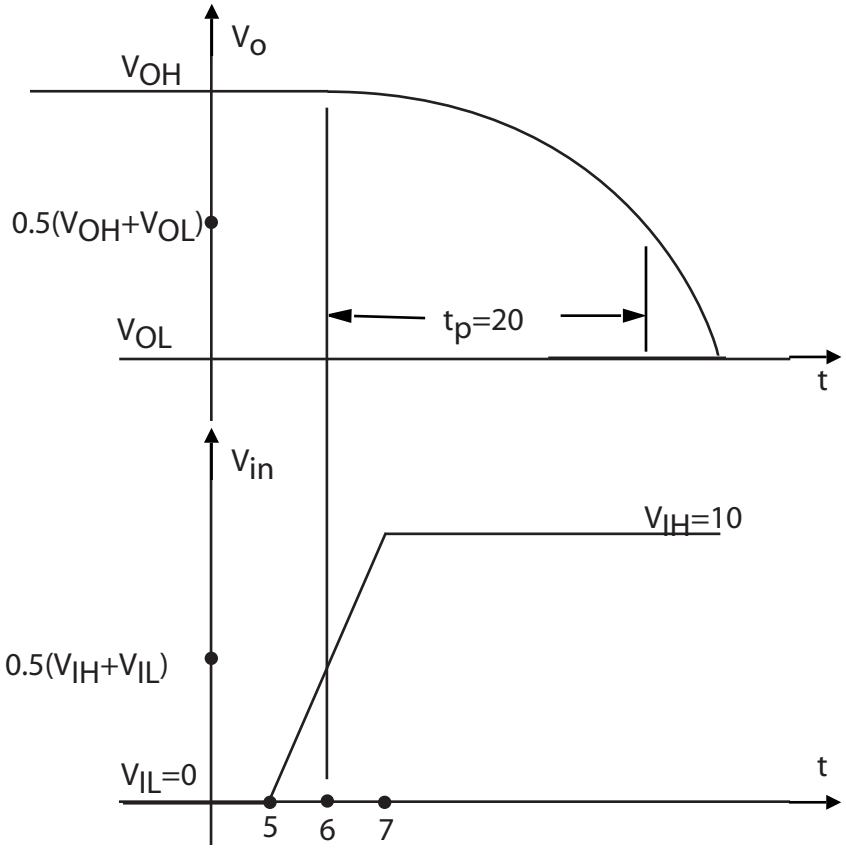
$v_{in} = 0$ for t < 5 μs

$v_{in} = 5(t - 5\ \mu s)$ for 5 μs < t < 7 μs

$v_{in} = 10$ for t > 7 μs

Solution

The input and the output response of the inverting comparator are shown in the figure.



Problem 8.1-04

Repeat Ex. 8.1-1 if the pole of the comparator is -10^5 radians/sec rather than -10^3 radians/sec.

Solution

The pole location is

$$\omega_c = -100 \text{ Krad/s}$$

$$k = \frac{V_{in}}{V_{in}(\min)} = \frac{10m}{0.1m} = 100$$

The propagation delay is given by

$$t_p = \frac{1}{\omega_c} \ln\left(\frac{2k}{2k-1}\right)$$

or, $$t_p = 50.1 \text{ ns} \quad (1)$$

Considering the maximum slew rate, the propagation delay can be expressed as

$$t_p' = \frac{V_{OH} - V_{OL}}{2SR}$$

or, $$t_p' = 500 \text{ ns} \quad (2)$$

From Equations (1) and (2), the propagation delay is

$$t_p = \underline{\underline{500 \text{ ns}}}$$

Problem 8.1-05

What value of V_{in} in Ex. 8.1-1 will give a slewing response?

Solution

The comparator will start to slew when the propagation delay of the comparator is dominated by its maximum slew rate (and not by the comparator's small-signal propagation delay).

$$\frac{V_{OH} - V_{OL}}{2SR} > \frac{1}{\omega_c} \ln\left(\frac{2k}{2k-1}\right)$$

or, $$\ln\left(\frac{2k}{2k-1}\right) < \frac{\omega_c (V_{OH} - V_{OL})}{2SR}$$

Solving for k, we get

$$k > 1000.5$$

or, $$V_{in} > \underline{\underline{100.05 \text{ mV}}}$$

Problem 8.2-01

Repeat Ex. 8.2-1 for the two-stage comparator of Fig. 8.2-5.

Solution

The output swing levels are

$$V_{OH} = V_{DD} - (V_{DD} - V_{G6}(\min) - |V_{TP}|)\left[1 - \sqrt{1 - \frac{2I_7}{\beta_6 (V_{DD} - V_{G6}(\min) - |V_{TP}|)^2}}\right]$$

or, $$V_{OH} = 2.5 - (2.5 - 0 - 0.7)\left[1 - \sqrt{1 - \frac{2(234)}{(50)(38)(2.5 - 0 - 0.7)^2}}\right]$$

or, $V_{OH} = \underline{2.43 \text{ V}}$

$V_{OL} = -V_{SS} = \underline{-2.5 \text{ V}}$

The minimum input resolution is

$$V_{in}(\min) = \frac{V_{OH} - V_{OL}}{A_v}$$

and, $$A_v = \frac{g_{m1} g_{m2}}{I_1 I_6 (\lambda_P + \lambda_N)^2} = 3300$$

or, $V_{in}(\min) = \underline{1.5 \text{ mV}}$

The pole locations are

$$p_1 = \frac{g_{ds2} + g_{ds4}}{C_I} = \underline{1.074 \text{ MHz}}$$

$$p_2 = \frac{g_{ds6} + g_{ds7}}{C_{II}} = \underline{0.67 \text{ MHz}}$$

Problem 8.2-02

If the poles of a two-stage comparator are both equal to -10^7 radians/sec., find the maximum slope and the time it occurs if the magnitude of the input step is $10V_{in}$(min) and V_{OH}-V_{OL} = 1V. What must be the *SR* of this comparator to avoid slewing?

Solution

The response to a step response to the above comparator can be written as,

$$v_{out}' = 1 - e^{-tn} - t_n e^{-tn} \qquad \text{where } v_{out}' = \frac{v_{out}}{A_v(0)V_{in}} \text{ and } t_n = tp_1$$

To find the maximum slope, differentiate twice and set to zero.

$$\frac{dv_{out}'}{dt_n} = e^{-tn} + t_n e^{-tn} - e^{-tn} = t_n e^{-tn}$$

$$\frac{d^2v_{out}'}{dt_n^2} = -t_n e^{-tn} + e^{-tn} = 0 \quad \Rightarrow \quad (1-t_n)e^{-tn} = 0 \quad \Rightarrow \quad t_n(\max) = tp_1 = 1$$

$\therefore$ $t_n(\max) = 1\text{sec}$ and $t(\max) = \frac{t_n}{|p_1|} = \frac{1}{10^7} = \underline{\underline{0.1\mu s}}$

$$\frac{dv_{out}'(\max)}{dt_n} = e^{-1} = 0.3679 \text{ V/sec} \quad \text{or} \quad \frac{dv_{out}'(\max)}{dt_n} = 3.679\text{V}/\mu\text{s}$$

$$\frac{dv_{out}'(\max)}{dt} = 10(V_{OH}-V_{OL})\cdot\frac{dv_{out}'(\max)}{dt_n} = \underline{\underline{36.79\text{V}/\mu\text{s}}}$$

$\therefore$ Therefore, the slew rate of the comparator should be greater than 36.79V/μs to avoid slewing.

Problem 8.2-03

Repeat Ex. 8.2-3 if p_1 = -5x10^6 radians/sec. and p_2 = 10x10^6 radians/sec.

Solution

Given $p_1 = -5$ Mrad/s, and $p_2 = -10$ Mrad/s

So, $m = \frac{p_2}{p_1} = 2$

When $V_{in} = 10m$

$$k = \frac{V_{in}}{V_{in}(\min)} = 15.576 \qquad \text{and,} \quad t_p = \frac{1}{p_1\sqrt{mk}} = 35.8 \text{ ns}$$

When $V_{in} = 100m$ (assuming no slewing)

$$k = \frac{V_{in}}{V_{in}(\min)} = 155.76 \qquad \text{and,} \quad t_p = \frac{1}{p_1\sqrt{mk}} = 11.3 \text{ ns}$$

When $V_{in} = 1$ (assuming no slewing)

$$k = \frac{V_{in}}{V_{in}(\min)} = 1557.6 \qquad \text{and,} \quad t_p = \frac{1}{p_1\sqrt{mk}} = 3.58 \text{ ns}$$

Problem 8.2-04

For Fig. 8.2-5, find all of the possible initial states listed in Table 8.2-1 of the first stage output voltage and the comparator output voltage.

Solution

Condition: $V_{G1} > V_{G2}, I_1 < I_{SS}, I_2 > 0$

$2.1315 < V_{o1} < 2.5$, and $V_{o2} = -2.5$

Condition: $V_{G1} >> V_{G2}, I_1 = I_{SS}, I_2 = 0$

$V_{o1} = 2.5$, and $V_{o2} = -2.5$

Condition: $V_{G1} < V_{G2}, I_1 > 0, I_2 < I_{SS}$

$V_{S2} < V_{o1} < V_{S2} + 0.3$, and $V_{o2} = 2.5 - \dfrac{0.123}{(2.5 - V_{o1} - 0.7)}$

Condition: $V_{G1} << V_{G2}, I_1 = 0, I_2 = I_{SS}$

$V_{o1} = -2.5$, and $V_{o2} = 2.47$

Condition: $V_{G2} > V_{G1}, I_1 > 0, I_2 < I_{SS}$

$V_{S2} < V_{o1} < V_{S2} + 0.3$, and $V_{o2} = 2.5 - \dfrac{0.123}{(2.5 - V_{o1} - 0.7)}$

Condition: $V_{G2} >> V_{G1}, I_1 = 0, I_2 = I_{SS}$

$V_{o1} = -2.5$, and $V_{o2} = 2.47$

Condition: $V_{G2} < V_{G1}, I_1 < I_{SS}, I_2 > 0$

$2.1315 < V_{o1} < 2.5$, and $V_{o2} = -2.5$

Condition: $V_{G2} << V_{G1}, I_1 = I_{SS}, I_2 = 0$

$V_{o1} = 2.5$, and $V_{o2} = -2.5$

Problem 8.2-05

Calculate the trip voltage for the comparator shown in Fig. 8.2-4. Use the parameters given in Table 3.1-2. Also, $(W/L)_2 = 100$ and $(W/L)_1 = 10$. $V_{BIAS} = 1$V, $V_{SS} = 0$V, and $V_{DD} = 4$ V.

Solution

Given, $V_{BIAS} = 1$, $V_{DD} = 4$, $V_{SS} = 0$, $S_7 = 100$, and $S_7 = 10$

The trip point is given by

$$V_{TRP} = V_{DD} - |V_{T6}| - \sqrt{\frac{K_N' S_7}{K_P' S_6}}(V_{BIAS} - V_{SS} - V_{T7})$$

or, $V_{TRP} = 1.89$ V

Problem 8.2-06

Using Problem 8.2-5, compute the worst-case variations of the trip voltage assuming a ±10% variation on V_T, K', V_{DD}, and V_{BIAS}.

Solution

The trip point is given by

$$V_{TRP} = V_{DD} - |V_{T6}| - \sqrt{\frac{K'_N S_7}{K'_P S_6}}(V_{BIAS} - V_{SS} - V_{T7})$$

The maximum trip point can be given by

$$V_{TRP}(\max) = 1.1V_{DD} - 0.9|V_{T6}| - \sqrt{\frac{0.9K'_N S_7}{1.1K'_P S_6}}(0.9V_{BIAS} - V_{SS} - 1.1V_{T7})$$

or, $V_{TRP}(\max) = \underline{\underline{3.22\ \text{V}}}$

The minimum trip point can be given by

$$V_{TRP}(\min) = 0.9V_{DD} - 1.1|V_{T6}| - \sqrt{\frac{1.1K'_N S_7}{0.9K'_P S_6}}(1.1V_{BIAS} - V_{SS} - 0.9V_{T7})$$

or, $V_{TRP}(\min) = \underline{\underline{0.39\ \text{V}}}$

Problem 8.2-07

Sketch the output response of the circuit in Problem 5, given a step input that goes from 4 to 1 volts. Assume a 10 pF capacitive load. Also assume the input has been at 4 volts for a very long time. What is the delay time from the step input to when the output changes logical (CMOS) states?

Solution

Let us assume $V_{OH} = 5$ V and $V_{OL} = 0$ V

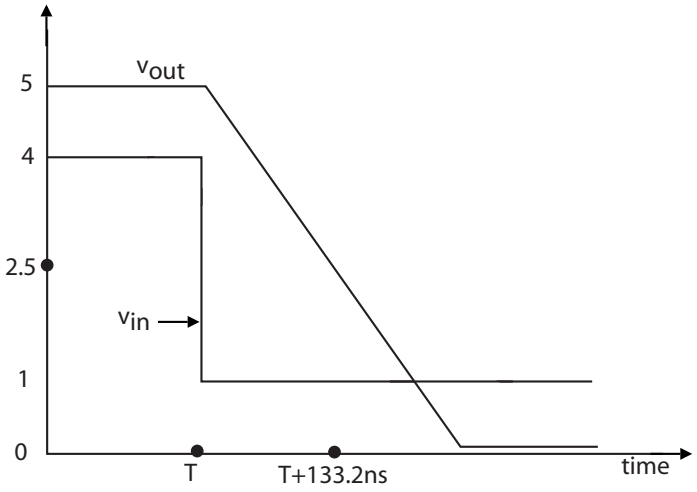
The trip point of the second stage is 3.965 V.

When the input makes a transition from 4 V to 1,

$$t_{ro1} = (0.2p)\frac{(3.965 - 0)}{30\mu} = 26.4$$

nsand $t_{f,out} = (10p)\frac{(2.5)}{234\mu} = 106.8$

ns



Thus, the total propagation delay is 133.2 ns. This is also the time it takes to change the output logical states.

Problem 8.2-08

Repeat Ex. 8.2-5 with v_{G2} constant and the waveform of Fig. 8.2-6 applied to v_{G1}.

Solution

Output fall time, t_r:

The initial states are $v_{o1} \approx$ -2.5V and $v_{out} \approx$ 2.5V. The reasoning for v_{o1} is interesting and should be understood. When V_{G1} = -2.5V and V_{G2} = 0V, the current in M1 is zero. This means the current is also zero in M4. Therefore, v_{o1} goes very negative and as M2 acts like a switch with $V_{DS} \approx 0$. Since the only current for M3 comes through M2 and from C_I, the voltage across M3 eventually collapses and I_3 becomes zero which causes $v_{o1} \approx$ -2.5V.

From Example 8.2-5, the trip point of the second stage is 1.465V, therefore the rise time of the first stage is,

$$t_{r1} = 0.2\text{pF}\left(\frac{1.465+2.5}{30\mu\text{A}}\right) = 26.4\text{ns}$$

The fall time of the second stage is found in Example 8.2-5 and is t_{f2} = 53.4ns. The total output fall time is

$$\therefore \quad t_r = t_{r1} + t_{f2} = \underline{\underline{79.8\text{ns}}}$$

Output rise time, t_r:

The initial states for this analysis are $v_{o1} \approx$ 2.5V and $v_{out} \approx$ -2.5V.

The input stage fall time is,

$$t_{f1} = 0.2\text{pF}\left(\frac{2.5\text{-}1.465}{30\mu\text{A}}\right) = 6.9\text{ns}$$

The output stage rise time is found by determining the best guess for V_{G6}. Since V_{G6} is going from 1.465 to –2.5V, let us approximate V_{G6} as

$$V_{G6} \approx 0.5(1.465\text{-}2.5) = -0.5175 \qquad \Rightarrow \qquad V_{SG6} = 2.5\text{-}(-0.5175) = 3.0175\text{V}$$

$$\therefore \quad I_6 = \frac{1}{2}K_P'\left(\frac{W_6}{L_6}\right)(V_{SG6}\text{-}|V_{TP}|)^2 = 0.5\cdot 50\text{x}10^{-6}\cdot 38(3.0175\text{-}0.7)^2 = 5102\mu\text{A}$$

$$t_{r2} = 5\text{pF}\left(\frac{2.5}{5102\mu\text{A}\text{-}234\mu\text{A}}\right) = 2.6\text{ns}$$

The total output rise time is,

$$\therefore \quad t_r = t_{f1} + t_{r2} = \underline{\underline{9.5\text{ns}}}$$

The propagation time delay of the comparator is,

$$t_p = t_r + t_r = \underline{\underline{44.7\text{ns}}}$$

Problem 8.2-09

Repeat Ex. 8.3-5 using the two-stage op amp designed in Ex. 6.3-1 if the compensation capacitor is removed.

Solution

Let us assume the initial states as

$V_{G2} = -2.5$ V

$V_{o1} = 2.5$ V

$V_{out} = -2.5$ V

and, $C_I = 0.2$ pF

For the rising edge of the input, $V_{G2} = 2.5$ V

$$V_{TRP2} = V_{DD} - \left(|V_{T6}| + \sqrt{\frac{2I_7}{K_P' S_6}} \right) \qquad \rightarrow \qquad V_{TRP2} = 1.6 \text{ V}$$

Thus, $\boxed{t_{fo1} = (0.2p)\frac{(0.9V)}{(30\mu)} = 6 \text{ ns}}$

The minimum value of V_{G6} is

$V_{G6} \cong -V_{GS2} = -1$ V

Average value of V_{G6} is

$$V_{G6} = \frac{-1 + 1.6}{2} = 0.3 \text{ V}$$

Thus, $I_6 = \frac{K_P' S_6}{2}(V_{SG6} - |V_{T6}|)^2 \qquad \rightarrow \qquad I_6 = 5.2875$ mA

So, $\boxed{t_{r,out} = (5p)\frac{(1.6 - (-2.5))}{(5287.5\mu)} = 2.36 \text{ ns}}$

Thus, total propagation delay for the rising input is $\boxed{t_{p1} = 8.36 \text{ ns}}$

For the falling edge of the input, $V_{G2} = -2.5$ V

$\boxed{t_{ro1} = (0.2p)\frac{(1.6 - (-2.5))}{(30\mu)} = 27.3 \text{ ns}}$

and, $\boxed{t_{f,out} = (5p)\frac{(2.5)}{(95\mu)} = 131.6 \text{ ns}}$

Thus, total propagation delay for the falling input is $\boxed{t_{p2} = 158.9 \text{ ns}}$

The average propagation delay is 83.63 ns.

Problem 8.2-10

Repeat Ex. 8.2-6 if the propagation time is t_p = 25ns.

Solution

Given, $t_p = 25$ ns

Let, $m = 1, k = 10$

or, $$|p_1| = |p_2| = \frac{1}{t_p\sqrt{mk}} = 12.65 \text{ Mrad/s}$$

$$I_6 = I_7 = \frac{p_2 C_{II}}{(\lambda_P + \lambda_N)} = 752 \ \mu A$$

or, $$\boxed{\left(\frac{W}{L}\right)_6 = \frac{2I_6}{K_P'(V_{dsat6})^2} = 120}$$

and, $$\boxed{\left(\frac{W}{L}\right)_7 = \frac{2I_7}{K_N'(V_{dsat7})^2} = 55}$$

Now, $A_{v2} = 44.4$, and for $A_v = 4000$, we have $A_{v1} = 90.11$

In order to satisfy the propagation delay from the first stage, let us assume

$$I_1 = 40 \ \mu A$$

The corresponding propagation delay of the first stage becomes

$$t_{p1} = \frac{C_I(V_{OH} - V_{OL})}{2I_2} = 10 \text{ ns}$$

Now, $g_{m1} = A_{v1}(\lambda_P + \lambda_N)I_1$

or, $g_{m1} = 324.4 \ \mu S$

or, $$\boxed{\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 12}$$

Also, $V_{IC}(\min) = -1.25$ V, and $V_{GS1} = 0.946$ V.

Thus, $V_{dsat5} = 0.304$ V

or, $$\boxed{\left(\frac{W}{L}\right)_5 = 16}$$

Assuming a V_{SG3} = 1.2V gives,

$$\boxed{\frac{W_3}{L_3} = \frac{W_4}{L_4} = \frac{40}{50(1.2\text{-}0.7)^2} \approx 4}$$

Problem 8.2-11

Design a comparator given the following requirements: $P_{\text{diss}} < 2$ mW, $V_{DD} = 3$ V, $V_{SS} = 0$ V $C_{\text{load}} = 3$ pF, $t_{\text{prop}} < 1$ μs, input CMR = 1.5 – 2.5 V, $A_{v0} > 2200$, and output voltage swing within 1.5 volts of either rail. Use Tables 3.1-2 and 3.3-1 with the following exceptions: $\lambda = 0.04$ for a 5 μm device length.

Solution

The ICMR is given as 1.5-2.5 V. Let us assume that

$$\left(\frac{W}{L}\right)_1 = \left(\frac{W}{L}\right)_2 = 3 \text{ and } I_5 = 30 \ \mu A$$

Considering the minimum input common-mode range

$$V_{IC}(\min) = V_{SS} + V_{T1}(\max) + V_{dsat1} + V_{dsat5}$$

or, $V_{dsat5} = 0.35$ V $\rightarrow$ $\left(\frac{W}{L}\right)_1 = 4.5$

Considering the maximum input common-mode range

$$V_{IC}(\max) = V_{DD} + V_{T1}(\min) - V_{T3}(\max) - V_{dsat3}$$

or, $V_{dsat5} = 0.2$ V $\rightarrow$ $\left(\frac{W}{L}\right)_3 = \left(\frac{W}{L}\right)_4 = 15$

Let us assume $\left(\frac{W}{L}\right)_7 = 31.5$ and $I_7 = 210 \ \mu A$

From proper mirroring of the bias currents, we get

$$\left(\frac{W}{L}\right)_6 = 210$$

The value of $C_{gs6} \cong 348$ fF. Thus, let us assume $C_I = 0.5$ pF.

The small-signal gain for this comparator is 8189 V/V.

The total power dissipation is 0.81 mW.

The trip point of the second stage is

$$V_{TRP2} = 2.1 \text{ V}$$

For the rising edge of the input, referring to the procedure in Example 8.2-5, the propagation delay can be calculated as

$t_{fo1} = 15$ ns, $t_{r,out} = 2.4$ ns, and the total propagation delay $t_{p1} = 17.4$ ns

For the falling edge of the input, the propagation delay can be found as

$t_{ro1} = 35$ ns, $t_{f,out} = 21.4$ ns, and the total propagation delay $t_{p2} = 56.4$ ns

The average propagation delay is 36.9 ns, which is well below 1000 ns.

Problem 8.3-01

Assume that the dc current in M5 of Fig. 8.3-1 is 100μA. If $W_6/L_6 = 5(W_4/L_4)$ and $W_{10}/L_{10} = 5(W_3/L_3)$, what is the propagation time delay of this comparator if C_L = 10pF and $V_{DD} = -V_{SS}$ = 2V?

Solution

The quiescent bias currents are

$$I_6 = I_7 = 250 \ \ \mu A$$

Under large-signal swing conditions, the maximum sourcing and sinking currents are

$$I_6(\max) = 500 \ \ \mu A$$

$$I_7(\max) = 500 \ \ \mu A$$

Thus, the propagation delay can be given by

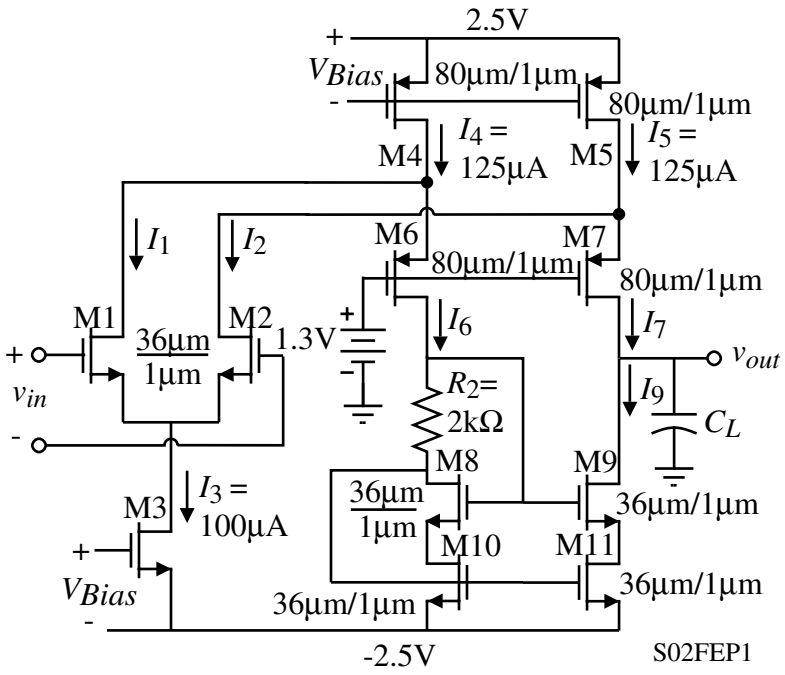
$$t_p = C_L \frac{0.5(V_{DD} - V_{SS})}{I_L}$$

or, $$t_p = (10p)\frac{0.5(2)}{(500\mu)}$$

or, $$t_p = \underline{\underline{20 \text{ ns}}}$$

Problem 8.3-02

If the folded-cascode op amp shown having a small-signal voltage gain of 7464V/V is used as a comparator, find the dominant pole if C_L = 5pF. If the input step is 10mV, determine whether the response is linear or slewing and find the propagation delay time. Assume the parameters of the NMOS transistors are K_N'=110V/μA^2, V_{TN} = 0.7V, λ_N=0.04V^{-1} and for the PMOS transistors are K_P'=110V/μA^2, V_{TP} = 0.7V, λ_P=0.04V^{-1}.



Solution

V_{OH} and V_{OL} can be found from many approaches. The easiest is simply to assume that V_{OH} and V_{OL} are 2.5V and –2.5V, respectively. However, no matter what the input, the values of V_{OH} and V_{OL} will be in the following range,

$$(V_{DD}\text{-}2V_{ON}) < V_{OH} < V_{DD} \quad \text{and} \quad V_{DD} < V_{OH} < (V_{SS}+2V_{ON})$$

The reasoning is as follows, suppose V_{in} >0. This gives I_1>I_2 which gives I_6<I_7 which gives I_9<I_7. V_{out} will increase until I_7 equals I_9. The only way this can happen is for M5 and M7 to leave saturation. The same reasoning holds for V_{in} <0.

Therefore assuming that V_{OH} and V_{OL} are 2.5V and –2.5V, respectively, we get

$$V_{in}(\text{min}) = \frac{5\text{V}}{7464} = 0.67\text{mV} \quad \rightarrow \quad k = \frac{10\text{mV}}{0.67\text{mV}} = 14.93$$

Problem 8.3-02 – Continued

The folded-cascode op amp as a comparator can be modeled by a single dominant pole. This pole is found as,

$$p_1 = \frac{1}{R_{out}C_L} \text{ where } R_{out} \approx g_{m9}r_{ds9}r_{ds11}\|[g_{m7}r_{ds7}(r_{ds2}\|r_{ds5})]$$

$g_{m9}=\sqrt{2\cdot 75\cdot 110\cdot 36}$ =771μS, $g_{ds9}=g_{ds11}=75\text{x}10^{-6}\cdot 0.04$ = 3μS, $g_{ds2}=50\text{x}10^{-6}(0.04)$=2μS

$g_{m7}=\sqrt{2\cdot 75\cdot 50\cdot 80}$ =775μS, $g_{ds5}=125\text{x}10^{-6}\cdot 0.05$ = 6.25μS, $g_{ds7}=50\text{x}10^{-6}(0.05)$=3.75μS

$$g_{m9}r_{ds9}r_{ds11} = (771\mu\text{S})\left(\frac{1}{3\mu\text{S}}\right)\left(\frac{1}{3\mu\text{S}}\right) = 85.67\text{M}\Omega$$

$$g_{m7}r_{ds7}(r_{ds2}\|r_{ds5} \approx (775\mu\text{S})\left(\frac{1}{3.75\mu\text{S}}\right)\left(\frac{1}{2\mu\text{S}}\|\frac{1}{6.25\mu\text{S}}\right) = 25.05\text{M}\Omega\ ,$$

$$R_{out} \approx 85.67\text{M}\Omega\|25.05\text{M}\Omega = 19.4\text{M}\Omega$$

The dominant pole is found as, $p_1 = \frac{1}{R_{out}C_L} = \frac{1}{19.4\text{x}10^6 5\text{pF}} = 10{,}318$ rps

The time constant is $\tau_1 = 96.9\mu$s.

For a dominant pole system, the step response is, $v_{out}(t) = A_{vd}(1\text{-}e^{-t/\tau_1})V_{in}$

The slope is the largest at $t = 0$. Evaluating this slope gives,

$\frac{dv_{out}}{dt} = \frac{A_{vd}}{\tau_1}e^{-t/\tau_1}V_{in}$ For $t = 0$, the slope is $\frac{A_{vd}}{\tau_1}V_{in} = \frac{7464}{96.9\mu\text{s}}(10\text{mV}) = 0.77\text{V}/\mu\text{s}$

The slew rate of this op amp/comparator is $SR = \frac{I_3}{C_L} = \frac{100\mu\text{A}}{5\text{pF}} = 20\text{V}/\mu\text{s}$

Therefore, the comparator does not slew and its propagation delay time is found from the linear response as,

$$t_P = \tau_1 \ln\left(\frac{2k}{2k\text{-}1}\right) = 96.9\mu\text{s}\cdot\ln\left(\frac{2\cdot 14.93}{2\cdot 14.93\text{-}1}\right) = (96.9\mu\text{s})(0.0341) = \underline{\underline{3.3\mu\text{s}}}$$

Problem 8.3-03

Find the open loop gain of Fig. 8.3-3 if the two-stage op amp is the same as Ex. 6.3-1 without the compensation and $W_{10}/L_{10} = 10(W_8/L_8) = 100(W_6/L_6)$, $W_9/L_9 = (K_{P'}/K_{N'})(W_8/L_8)$, $W_{11}/L_{11} = (K_{P'}/K_{N'})(W_{10}/L_{10})$ and the quiescent current in M8 and M9 is 100μA and in M10 and M11 is 500μA. What is the propagation time delay if C_{II} = 100pF and the step input is large enough to cause slewing?

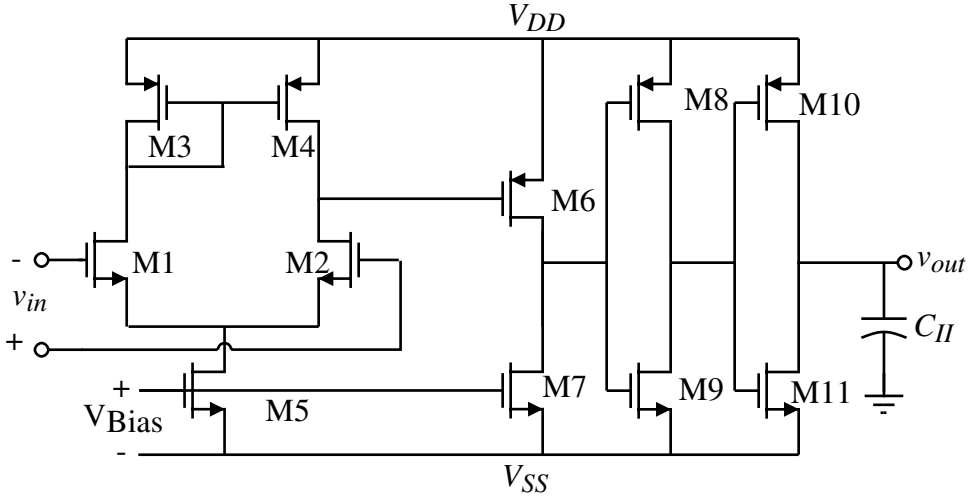


Figure 8.3-3 Increasing the capacitive drive of a two-stage, open-loop comparator.

Solution

From Ex. 6.3-1, we know that the small-signal gain to the input of the M8-M9 inverter is 7696 V/V. The gain of the M8-M9 and M10-M11 push-pull inverters are given as,

$$A_{v8,9} = -\frac{g_{m8} + g_{m9}}{g_{ds8} + g_{ds9}} \text{ and } \quad A_{v10,11} = -\frac{g_{m10} + g_{m12}}{g_{ds10} + g_{ds12}}$$

Since $W_6/L_6 = 94$ then $W_8/L_8 = 940$ and $W_9/L_9 = (50/110)940 = 427$.

Now, $g_{m8} = g_{m9} = \sqrt{2 \cdot 50 \cdot 940 \cdot 100}$ μS = 3,066μS, $g_{ds8} = 0.04 \cdot 100$μS = 4μS and $g_{ds9} = 0.05 \cdot 100$μS = 5μS.

$$\therefore A_{v8,9} = -\frac{3{,}066 + 3{,}066}{4+5} = -681.3 \text{ V/V}$$

Since $W_6/L_6 = 94 W_{10}/L_{10} = 9400$ and $W_{11}/L_{11} = (50/110)9400 = 4270$.

Now, $g_{m10} = g_{m12} = \sqrt{2 \cdot 50 \cdot 9400 \cdot 500}$ μS = 21.68mS, $g_{ds10} = 0.04 \cdot 500$μS = 20μS and $g_{ds9} = 0.05 \cdot 500$μS = 25μS.

$$\therefore A_{v10,11} = -\frac{21.68\text{x}2\text{x}10^3}{20+25} = -963.5 \text{ V/V} \Rightarrow \text{Total gain} = 7696 \cdot 681 \cdot 963 = \underline{\underline{5.052\text{x}10^9 \text{ V/V}}}$$

$$t_p = C\frac{\Delta V_o}{I} \text{ where } I = \frac{K_P W_{10}}{2L_{10}}(V_{SG10} - |V_{TP}|)^2 = 235\text{x}10^3(5-0.7)^2 = 4.345\text{A}$$

$$\therefore \quad t_p = 100\text{x}10^{-12}\left(\frac{2.5\text{V}}{4.345\text{A}}\right) = \underline{\underline{57.5 \text{ x}10^{-12} \text{ sec.}}}$$

Problem 8.3-04

Fig. P8.3-4 shows a circuit called a clamped comparator. Use the parameters of Table 3.1-2 and calculate the gain of this comparator. What is the positive and negative slew rate of this comparator if the load capacitance is 5 pF?

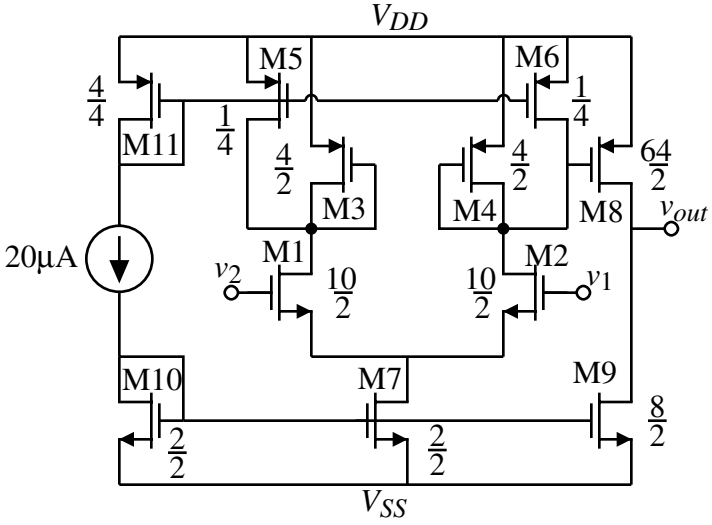


Fig. P8.3-4

Solution

$$I_7 = 20 \ \mu A$$

$$I_1 = I_2 = 10 \ \mu A$$

$$I_5 = I_6 = 5 \ \mu A$$

So, $I_3 = I_4 = 5 \ \mu A$

$$I_8 = 80 \ \mu A$$

The small-signal voltage gain is

$$A_v = \frac{g_{m2} g_{m8}}{2 g_{m4} (g_{ds8} + g_{ds9})}$$

or, $A_v = 83$ V/V

The negative slew rate is

$$SR^- = -\frac{I_9}{C_L} = \underline{\underline{-16 \text{V/μs}}}$$

To calculate the positive slew rate

$$V_{SG8}(\min) = |V_{T4}| + \sqrt{\frac{2I_4(\max)}{K_P S_4}}$$

or, $V_{SG8}(\min) = 0.7 + \sqrt{\frac{2(15\mu)}{(50\mu)(2)}} = 1.25$ V

So, $I_8(\max) = 242 \ \mu A$

or, $SR^+ = \frac{I_8(\max)}{C_L} = \underline{\underline{48.4 \text{V/μs}}}$

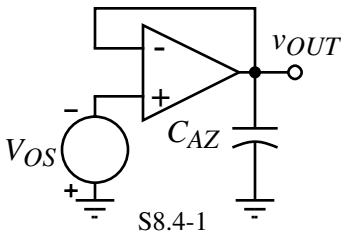
Problem 8.4-01

If the comparator used in Fig. 8.4-1 has a dominant pole at 10^4 radians/sec and a gain of 10^3, how long does it take C_{AZ} to charge to 99% of its final value, V_{OS}? What is the final value that the capacitor, C_{AZ}, will charge to if left in the configuration of Fig. 8.4-1(b) for a long time?

Solution

The output voltage for the circuit shown can be expressed as,

$$V_{out}(s) = (-V_{OS} - V_{out}(s)) \left(\frac{A_v(0)}{1 + \frac{s}{|p_1|}} \right)$$



S8.4-1

This can be solved for the transfer $V_{out}(s)/V_{OS}$ as follows,

$$\frac{V_{out}(s)}{V_{OS}(s)} = \frac{\frac{A_v(0)}{1 + \frac{s}{|p_1|}}}{1 + \frac{A_v(0)}{1 + \frac{s}{|p_1|}}} = \frac{A_v(0)}{1 + A_v(0) + \frac{s}{|p_1|}} = \frac{A_v(0)|p_1|}{s + (1 + A_v(0))\,|p_1|}$$

Assuming $V_{OS}(s)$ is a step function then,

$$V_{out}(s) = -\frac{V_{OS}}{s}\left(\frac{A_v(0)|p_1|}{s + (1 + A_v(0))\,|p_1|} \right) = -\frac{A_v(0)V_{OS}}{1 + A_v(0)}\left[\frac{1}{s} - \frac{1}{s + (1 + A_v(0)|p_1|)} \right]$$

Taking the inverse Laplace transform gives,

$$v_{out}(t) = -\frac{A_v(0)V_{OS}}{1 + A_v(0)}\left[1 - e^{-[1 + A_v(0)]|p_1|t} \right]$$

Let $v_{out}(t) = -0.99V_{OS}$ and solve for the time T.

$$v_{out}(t) = -0.99V_{OS} = -\frac{1000V_{OS}}{1000+1}\left[1 - e^{-1001 \cdot 10^4 T}\right]$$

$$1 - \frac{1001}{1000} \cdot \frac{99}{100} = 0.0090 = e^{-1001 \cdot 10^4 T} \Rightarrow \qquad 110.99 = e^{1001 \cdot 10^4 T}$$

$$\therefore \qquad T = 0.9990 \times 10^{-7}\, ln(110.99) = \underline{\underline{0.47\mu s}}$$

As $t \to \infty$, $v_{out}(t) \to -\frac{1000V_{OS}}{1000+1} = \underline{\underline{0.999V_{OS}}}$

Problem 8.4-02

Use the circuit of Fig. 8.4-9 and design a hysteresis characteristic that has $V_{TRP}^{-} = 0\text{V}$ and $V_{TRP}^{+} = 1\text{V}$ if $V_{OH} = 2\text{V}$ and $V_{OL} = 0\text{V}$. Let $R_1 = 100\text{k}\Omega$.

Solution

Given, $V_{TRP}^{+} = 1\text{ V}$

$V_{TRP}^{-} = 0\text{ V}$

$V_{OH} = 2\text{ V}$

$V_{OL} = 0\text{ V}$

and, $R_1 = 100\ K\Omega$

Now, $V_{TRP}^{+} = \left(\frac{R_1 + R_2}{R_2}\right) V_{REF} - \frac{R_1}{R_2} V_{OL}$

or, $\left(\frac{R_1 + R_2}{R_2}\right) V_{REF} = 1$ (1)

Also, $V_{TRP}^{-} = \left(\frac{R_1 + R_2}{R_2}\right) V_{REF} - \frac{R_1}{R_2} V_{OH}$

or, $\left(\frac{R_1 + R_2}{R_2}\right) V_{REF} = \frac{R_1}{R_2} 2$

From Equation (1)

$$\frac{R_1}{R_2} 2 = 1$$

or, $R_2 = 2R_1 = 200\ K\Omega$

and, $V_{REF} = \frac{2}{3}\text{ V}$

Problem 8.4-03

Repeat Problem 8.4-2 for Fig. 8.4-10.

Solution

Given, $V_{TRP}^{+} = 1$ V

$V_{TRP}^{-} = 0$ V

$V_{OH} = 2$ V

$V_{OL} = 0$ V

and, $R_1 = 100\ K\Omega$

Now, $V_{TRP}^{-} = \left(\frac{R_2}{R_1 + R_2}\right) V_{OL} + \left(\frac{R_2}{R_1 + R_2}\right) V_{REF}$

or, $V_{REF} = 0$ V

Also, $V_{TRP}^{+} = \left(\frac{R_2}{R_1 + R_2}\right) V_{OH} + \left(\frac{R_2}{R_1 + R_2}\right) V_{REF}$

or, $V_{TRP}^{+} = \left(\frac{R_2}{R_1 + R_2}\right) V_{OH}$

or, $R_1 = R_2 = 100\ K\Omega$

Problem 8.4-04

Assume that all transistors in Fig. 8.4-11 are operating in the saturation mode. What is the gain of the positive feedback loop, M6-M7 using the *W/L* values and currents of Ex. 8.4-2?

Solution

The loop-gain in the positive feedback loop can be expressed as

$$|LG| = \frac{g_{m6} g_{m7}}{\left(g_{m4} + g_{ds4} + g_{ds2} + g_{ds6}\right)\left(g_{m3} + g_{ds1} + g_{ds3} + g_{ds7}\right)}$$

Now, $S_1 = S_2 = S_6 = S_7 = 10$, and $S_3 = S_4 = 2$

$I_5 = 20\ \mu A$

So, $I_3 = \frac{10}{6}\ \mu A$, and $I_6 = \frac{50}{6}\ \mu A$

And, $g_{m6} = 91.3\ \mu S$

$g_{m7} = 91.3\ \mu S$

$g_{m3} = 18.3\ \mu S$

$g_{m4} = 18.3\ \mu S$

So, $|LG| = \underline{\underline{22.6}}$

Problem 8.4-05

Repeat Ex. 8.4-1 to design $V_{TRP}^{+} = - V_{TRP}^{-} = 0.5$V.

Solution

Given, $V_{TRP}^{+} = 0.5$ V

$V_{TRP}^{-} = -0.5$ V

$V_{OH} = 2$ V

$V_{OL} = -2$ V

Now, $$V_{TRP}^{-} = \left(\frac{R_2}{R_1 + R_2}\right)V_{OL} + \left(\frac{R_2}{R_1 + R_2}\right)V_{REF}$$

or, $$-0.5 = \left(\frac{R_2}{R_1 + R_2}\right)(-2) + \left(\frac{R_2}{R_1 + R_2}\right)V_{REF} \qquad (1)$$

Also, $$V_{TRP}^{+} = \left(\frac{R_2}{R_1 + R_2}\right)V_{OH} + \left(\frac{R_2}{R_1 + R_2}\right)V_{REF}$$

or, $$0.5 = \left(\frac{R_2}{R_1 + R_2}\right)(2) + \left(\frac{R_2}{R_1 + R_2}\right)V_{REF} \qquad (2)$$

Solving Equations (1) and (2), we get

$R_1 = 3R_2$, and $V_{REF} = 0$ V

Problem 8.4-06

Repeat Ex. 8.4-2 if i_5 = 50μA. Confirm using a simulator.

Solution

$$I_5 = 50 \ \ \mu A$$

$$S_1 = S_2 = 5\ ,\ S_6 = S_7 = 10\ ,\ \text{and}\ S_3 = S_4 = 2$$

To calculate the positive trip point

$$I_3 = \frac{50}{6} = 8.33 \ \ \mu A$$

$$I_2 = I_5 - I_1 = 50 - 8.33 = 41.67 \ \ \mu A$$

$$V_{GS1} = V_{T1} + \sqrt{\frac{2I_1}{K_N' S_1}} = 0.874 \ \ \text{V}$$

$$V_{GS2} = V_{T2} + \sqrt{\frac{2I_2}{K_N' S_2}} = 1.089 \ \ \text{V}$$

or, $V_{TRP}^{+} = V_{GS2} - V_{GS1} = \underline{\underline{0.215\text{V}}}$

Based on a similar analysis, the negative trip point will be

$$I_4 = \frac{50}{6} = 8.33 \ \ \mu A$$

$$I_1 = 41.67 \ \ \mu A$$

$$V_{GS2} = 0.874 \ \ \text{V}$$

$$V_{GS1} = 1.089 \ \ \text{V}$$

$$V_{TRP}^{-} = V_{GS2} - V_{GS1} = \underline{\underline{-0.215\text{V}}}$$

Problem 8.5-01

List the advantages and disadvantages of the switched capacitor comparator of Fig. 8.5-1 over an open-loop comparator having the same gain and frequency response.

Solution

	Advantages	Disadvantages
Fig. 8.5-1	Can remove input offset voltage Positive terminal on ground eliminates need for good ICMR	Requires switches Charge feedthrough Must be stable in autozero mode
Open-loop Comparator	Stability not of concern Continuous time operation	Requires good ICMR Can't remove input offset voltage

Problem 8.5-02

If the current and *W/L* values of the two latches in Fig. 8.5-3 are identical, which latch will be faster? Why?

Solution

The closed loop gain of the NMOS latch can be given by

$$A_{vn} = \left(\frac{g_m}{g_{ds}} \right)^2 = \sqrt{\frac{2K_N'(W/L)}{I\lambda_N^2}}$$

The closed loop gain of the PMOS latch can be given by

$$A_{vp} = \left(\frac{g_m}{g_{ds}} \right)^2 = \sqrt{\frac{2K_P'(W/L)}{I\lambda_P^2}}$$

It can be seen that

$$\frac{A_{vn}}{A_{vp}} = 3.4375$$

Thus, the NMOS latch would be faster (as it has larger small-signal loop gain).

Problem 8.5-03

Repeat Ex. 8.5-1 if $\Delta V_{out} = 0.5\text{V}(V_{OH}\text{-}V_{OL})$.

Solution

The propagation delay of the latch can be expressed as

$$t_p = \tau_L \ln\left(\frac{\Delta V_{out}}{\Delta V_{in}}\right)$$

where, $\tau_L = 108$ ns

or, $$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right)$$

When $\Delta V_{in} = 0.01(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{422 \text{ ns}}$$

When $\Delta V_{in} = 0.1(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{174 \text{ ns}}$$

Problem 8.5-04

Repeat Ex. 8.5-1 if the dc latch current is 50μA.

Solution

$g_m = 332$ μS

$g_{ds} = 2$ μS

So, the latch gain is

$A_v = 166$ V/V

The latch time constant is given by

$$\tau_L = 0.67 C_{ox} \sqrt{\frac{WL^3}{2K_N I}} = 48 \text{ ns}$$

When, $V_{in} = 0.01(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{188 \text{ ns}}$$

When, $V_{in} = 0.1(V_{OH} - V_{OL})$

$$t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2\Delta V_{in}}\right) = \underline{76.8 \text{ ns}}$$

Problem 8.5-05

Redevelop the expression for $\Delta V_{out}/\Delta V_i$ for the circuit of Fig. P8.5-5 where $\Delta v_{out} = v_{o2} - v_{o1}$ and $\Delta V_i = v_{i1} - v_{i2}$.

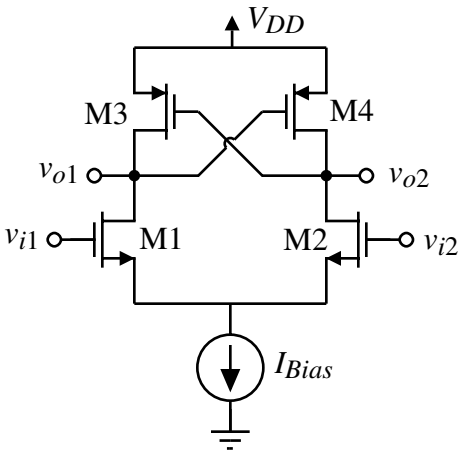


Figure P8.5-5

Solution

Referring to the figure and applying nodal analysis

$$g_{m1}v_{i1} + g_{ds1}v_{o1} + g_{m3}v_{o2} + g_{ds3}v_{o1} = 0$$

or,

$$g_{m1}v_{i1} + (g_{ds1} + g_{ds3})v_{o1} + g_{m3}v_{o2} = 0 \qquad (1)$$

Similarly, applying nodal analysis

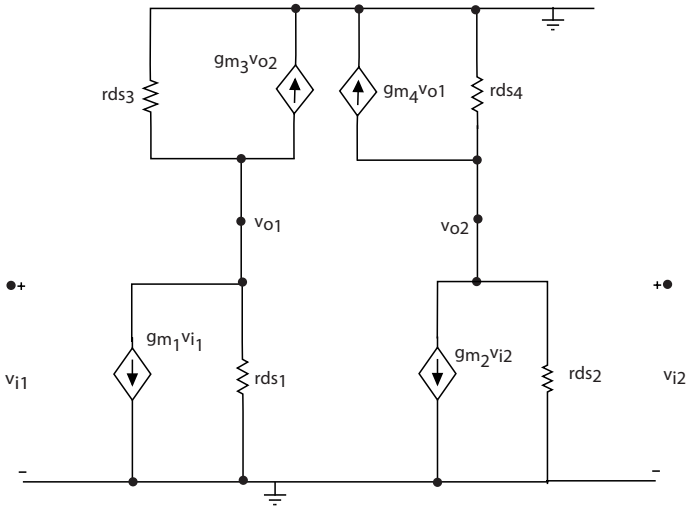
$$g_{m2}v_{i2} + (g_{ds2} + g_{ds4})v_{o2} + g_{m4}v_{o1} = 0 \qquad (2)$$

Subtracting Equation (2) from Equation (1), we get

$$g_{m1}(v_{i1} - v_{i2}) = (-g_{m3} + g_{ds1} + g_{ds3})(v_{o2} - v_{o1})$$

or,

$$\frac{(v_{o2} - v_{o1})}{(v_{i1} - v_{i2})} = \frac{g_{m1}}{(-g_{m3} + g_{ds1} + g_{ds3})}$$



Problem 8.5-06

Compare the dynamic latch of Fig. 8.5-8 with the NMOS and PMOS latches of Fig. 8.5-3.

Solution

	Advantages	Disadvantages
Fig. 8.5-3	Work with smaller power supply	Class A output – can't source and sink with the same current-slow
Fig. 8.5-8	Push-pull is good for sinking and sourcing a lot of current -fast	Needs larger power supply

Problem 8.5-07

Use the worst case values of the transistor parameters in Table 3.1-2 and calculate the worst case voltage offset for the NMOS latch of Fig. 8.5-3(a).

Solution

The offset voltage can be expressed as

$$|V_{OS}| = |V_{o2} - V_{o1}| = |V_{T1} + V_{dsat1} - V_{T2} - V_{dsat2}|$$

or, $$|V_{OS}| = \left[2\Delta V_T + \sqrt{\frac{2I_1}{K_1' S_1}} - \sqrt{\frac{2I_2}{K_2' S_2}} \right]$$

Assuming, $I_1 = I_2 = 10 \ \mu A$, and $S_1 = S_2 = 10$

$$|V_{OS}| = \left[2(0.15) + \sqrt{\frac{2(10\mu)}{0.9(110\mu)(10)}} - \sqrt{\frac{2(10\mu)}{1.1(110\mu)(10)}} \right]$$

or, $|V_{OS}| = 0.314$ V

Problem 8.6-01

Assume an op amp has a low frequency gain of 1000 V/V and a dominant pole at -10^4 radians/sec. Compare the -3dB bandwidths of the configurations in Fig. P8.6-1(a) and (b) using this op amp.

Solution

Given, $A_v(0) = 1000$, and $p_1 = 10$ Krad/s

Thus, the gain-bandwidth frequency is

$$GB = A_v(0) p_1 = 10 \text{ Mrad/s}$$

a) The closed-loop gain is (-25). Thus, the –3 dB bandwidth becomes

$$\omega_{-3dB} = \frac{GB}{25} = 400 \text{ Krad/s}$$

b) The closed-loop gain of each gain stage is (-5). Thus, the –3 dB bandwidth becomes

$$\omega_{-3dB} = \frac{GB}{5} = 2000 \text{ Krad/s}$$

There would be two poles at 2 Mrad/s at the output; each being created by a single gain stage.

Problem 8.6-02

What is the gain and -3dB bandwidth (in Hz) of Fig. P8.6-2 if C_L = 1pF? Ignore reverse bias voltage effects on the pn junctions and assume the bulk-source and bulk-drain areas are given by W x5μm.

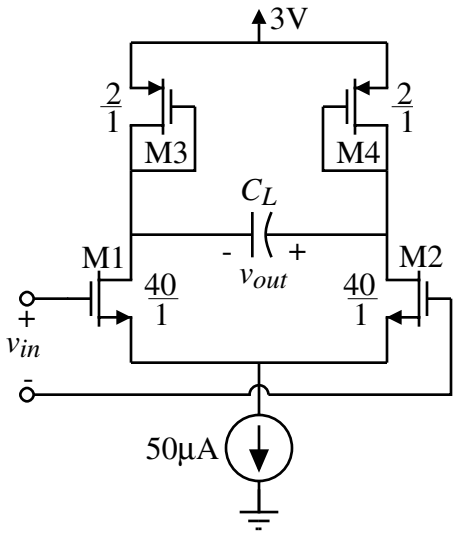


Fig. P8.6-2

Solution

$$A_v = \frac{g_{m1}}{g_{m3}} = \sqrt{\frac{K_N' S_1}{K_P' S_3}} = 6.6 \text{ V/V}$$

The single-ended output resistance is

$$R_o = \frac{1}{g_{m3}} = 14.14 \text{ K}\Omega$$

The pole frequency at the output is given by

$$p_1 = -\frac{1}{R_o\left(2C_L + C_{gs3} + C_{bd3} + C_{gd1} + C_{bd1}\right)}$$

or, $$p_1 \cong -\frac{1}{R_o\left(2C_L + C_{bd1}\right)}$$

or, $p_1 = -5.15$ MHz $\rightarrow f_{\text{-3dB}} = \underline{\underline{5.15 \text{ MHz}}}$

Problem 8.6-03

What is the gain and -3dB bandwidth (in Hz) of Fig. P8.6-3 if C_L = 1pF? Ignore reverse bias voltage effects on the pn junctions and assume the bulk-source and bulk-drain areas are given by W x5µm. The W/L ratios for M1 and M2 are 10µm/1µm and for the remaining PMOS transistors the W/L ratios are all 2µm/1µm.

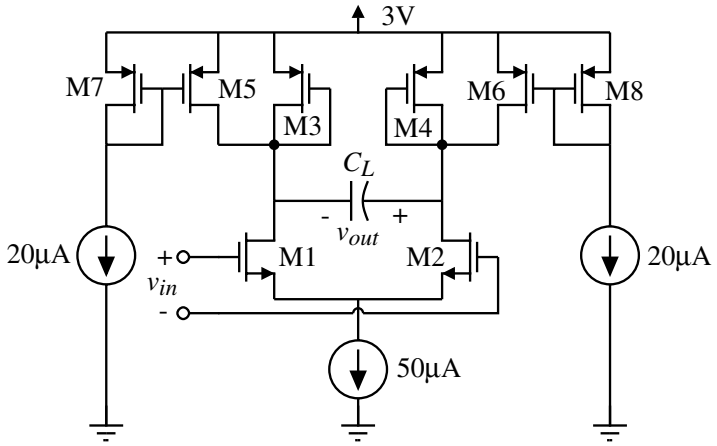
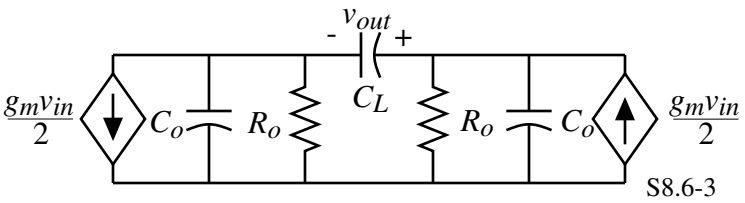


Fig. P8.6-3

Solution

A small-signal model which can be used to solve this problem is shown.



S8.6-3

The voltage gain and the –3dB bandwidth can be expressed as,

$$\frac{v_{out}}{v_{in}} = g_m R_o \quad \text{and} \quad \omega_{-3dB} = \frac{1}{(C_L+0.5C_o)2R_o}$$

The various values in the above relationships are:

$$g_m = \sqrt{2\cdot K_N(W_1/L_1)I_{D1}} = \sqrt{2\cdot 110\cdot 10\cdot 25}\ \mu S = 234.5\mu S$$

$$R_o \approx \frac{1}{g_{m3}} \| r_{ds1} \| r_{ds3} \| r_{ds5}, \quad g_{m3} = \sqrt{2\cdot K_P(W_1/L_1)I_{D3}} = \sqrt{2\cdot 50\cdot 2\cdot 5}\ \mu S = 31.62\mu S$$

$$r_{ds1} = \frac{1}{0.04\cdot 25\mu A} = 1M\Omega,\ r_{ds3} = \frac{1}{0.05\cdot 5\mu A} = 4M\Omega \text{ and } r_{ds5} = \frac{1}{0.04\cdot 20\mu A} = 0.8M\Omega$$

$$\therefore\ R_o = 31.623k\Omega \| 1M\Omega \| 4M\Omega \| 0.8M\Omega = 29.31k\Omega$$

$$C_o \approx C_{gs3}+C_{bd1}+C_{bd3}+C_{bd5} \qquad C_{gs3} = CGSO\cdot W_5 + 0.67\cdot C_{ox}\cdot W_5\cdot L_5$$

$$= 220x10^{-12}F/m\cdot 2x10^{-6}m + 0.67\cdot 24.7x10^{-4}F/m^2\cdot 2x10^{-12}m^2 = 3.73fF$$

$$C_{bd1} = CJ\cdot AS + CJSW\cdot PS = 770x10^{-6}F/m^2\cdot 50x10^{-12}m^2 + 380x10^{-12}F/m\cdot 30x10^{-6}m$$

$$= 38.5fF + 11.4fF = 49.9fF$$

$$C_{bd3} = C_{bd5} = 560x10^{-6}F/m^2\cdot 10x10^{-12}m^2 + 350x10^{-12}F/m\cdot 14x10^{-6}m = 10.5fF$$

$$\therefore\ C_o = 74.6fF \rightarrow \omega_{-3dB} = \frac{1}{(1.073pF)58.62k\Omega} = 16.445x10^6 rads/sec$$

Finally, $f_{-3dB} = \underline{\underline{2.62MHz}}$ and $A_v = \underline{\underline{6.873V/V}}$

Problem 8.6-04

Assume that a comparator consists of an amplifier cascaded with a latch. Assume the amplifier has a gain of 5V/V and a -3dB bandwidth of $1/\tau_L$, where τ_L is the latch time constant and is equal to 10ns. Find the propagation time delay for the overall configuration if the applied input voltage is $0.05(V_{OH}\text{-}V_{OL})$ and the voltage applied to the latch from the amplifier is (a) $\Delta V_i = 0.05(V_{OH}\text{-}V_{OL})$, (b) $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$, (c) $\Delta V_i = 0.15(V_{OH}\text{-}V_{OL})$ and (d) $\Delta V_i = 0.2(V_{OH}\text{-}V_{OL})$. Assume that the latch is enabled as soon as the output of the amplifier is equal to $0.05(V_{OH}\text{-}V_{OL})$. From your results, what value of ΔV_i would give minimum propagation time delay?

Solution

The transfer function of the amplifier is $A_v(s) = \dfrac{A_v(0)}{s\tau_L+1}$

The output voltage of the amplifier is $v_o(t) = A_v(0)[1\text{-}e^{-t/\tau_L}]\Delta V_i$

Let $\Delta V_i = x\cdot(V_{OH}\text{-}V_{OL})$, therefore the delay of the amplifier can be found as

$$x(V_{OH}\text{-}V_{OL}) = A_v(0)[1\text{-}e^{-t1/\tau_L}]0.05(V_{OH}\text{-}V_{OL}) = 5[1\text{-}e^{-t1/\tau_L}]0.05(V_{OH}\text{-}V_{OL})$$

or

$$x = 0.25[1\text{-}e^{-t1/\tau_L}] \quad \rightarrow \quad t_1 = \tau_L\, ln\left(\frac{1}{1\text{-}4x}\right)$$

The delay of the latch can be found as

$$t_2 = \tau_L\, ln\left(\frac{V_{OH}\text{-}V_{OL}}{2x(V_{OH}\text{-}V_{OL})}\right) = \tau_L\, ln\left(\frac{1}{2x}\right)$$

The propagation time delay of the comparator can be expressed in terms of x as,

$$t_p = t_1+t_2 = \tau_L\, ln\left(\frac{1}{1\text{-}4x}\right) + \tau_L\, ln\left(\frac{1}{2x}\right) = \tau_L\, ln\left(\frac{1}{2x\text{-}8x^2}\right)$$

Thus,

$x = 0.05 = 1/20 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 2.23\text{ns}+2.30\text{ns} =$ <u>25.26ns</u>

$x = 0.1 = 1/10 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 5.11\text{ns}+16.09\text{ns} =$ <u>21.20ns</u>

$x = 0.15 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 9.16\text{ns}+12.04\text{ns} =$ <u>21.20ns</u>

$x = 0.2 = 1/5 \quad \Rightarrow \quad \tau_p = t_1 + t_2 = 16.09\text{ns}+9.16\text{ns} =$ <u>25.26ns</u>

Note that differentiating t_p with respect to x and setting to zero gives

$$x_{min} = 1/8 = 0.125$$

Therefore, minimum delay of <u>20.08ns</u> is achieved when <u>$x = 1/8$</u>.

Problem 8.6-05

Assume that a comparator consists of two identical amplifiers cascaded with a latch. Assume the amplifier has the characteristics given in the previous problem. What would be the normalized propagation time delay if the applied input voltage is $0.05(V_{OH}\text{-}V_{OL})$ and the voltage applied to the latch is $\Delta V_i = 0.1(V_{OH}\text{-}V_{OL})$?

Solution

The transfer function of the amplifiers is $A_v(s) = \left(\frac{A_v(0)}{s\tau_L+1}\right)^2 = \left(\frac{5}{s\tau_L+1}\right)^2$

The output voltage of the amplifiers is

$$V_o(s) = \frac{\frac{25}{\tau_L{}^2}}{(s+1/\tau_L)^2}\cdot\frac{0.05(V_{OH}\text{-}V_{OL})}{s} = \frac{1.25(V_{OH}\text{-}V_{OL})}{\tau_L{}^2}\left[\frac{a}{s} + \frac{b}{s+(1/\tau_L)} + \frac{c}{(s+(1/\tau_L))^2}\right]$$

or $$H(s) = \frac{1}{s(s+(1/\tau_L))^2} = \frac{a}{s} + \frac{b}{s+(1/\tau_L)} + \frac{c}{(s+(1/\tau_L))^2}$$

Solving for a, b, and c, by partial fraction expansion gives

$$a = sH(s)\Big|_{s=0} = \tau_L{}^2, \quad c = [s+(1/\tau_L)]^2\cdot H(s)\Big|_{s=-1/\tau_L} = -\tau_L$$

and $$\frac{d}{da}\left[\frac{1}{s} = a[s+(1/\tau_L)]^2 + b[s+(1/\tau_L)] + c\right] \Rightarrow -\frac{1}{s^2} = 2a[s+(1/\tau_L)] + b$$

$\therefore$ Let s=-1/τ_L to get $b = -\tau_L{}^2$

$$V_o(s) = 1.25(V_{OH}\text{-}V_{OL})\left[\frac{1}{s} - \frac{1}{s+(1/\tau_L)} - \frac{\tau_L}{[s+(1/\tau_L)]^2}\right]$$

Taking the inverse Laplace transform gives,

$$v_o(t) = 1.25(V_{OH}\text{-}V_{OL})\left[1 - e^{-t/\tau_L} - \frac{t}{\tau_L}e^{-t/\tau_L}\right]$$

Setting $v_o(t) = 0.05(V_{OH}\text{-}V_{OL})$ and solving for the amplifier delay, t_1, gives

$$\frac{t_1}{\tau_L} = ln\left[\frac{1.25}{1.2} + \frac{1.25}{1.2}\frac{t_1}{\tau_L}\right] = ln\left[1.041667\left(1+\frac{t_1}{\tau_L}\right)\right]$$

Solving iteratively gives $t_1/\tau_L = 0.313$ $\Rightarrow$ $t_1 = 3.13$ns

The latch delay time, t_2 is found as

$$t_2 = \tau_L ln\left(\frac{V_{OH}\text{-}V_{OL}}{2\text{x}0.1(V_{OH}V_{OL})}\right) = 10\text{ns}\ ln(5) = 16.095\text{ns}$$

$\therefore$ $t_{comparator} = t_1 + t_2 = \underline{\underline{19.226\text{ns}}}$

Problem 8.6-06

Repeat Problem 5 if there are three identical amplifiers cascaded with a latch. What would be the normalized propagation time delay if the applied input voltage is $0.05(V_{OH}\text{-}V_{OL})$ and the voltage applied to the latch is $\Delta V_i = 0.2(V_{OH}\text{-}V_{OL})$?

Solution

The combined transfer function of the three, cascaded amplifier stage can be given as

$$A_v(s) = \frac{A_v^3}{\left(1 + s/p\right)^3}$$

In response to a step input, the output response of the three, cascaded amplifier stages can be approximated as

$$v_{oa}(t) = A_v^3 v_{in}\left(1 - 3e^{-t/\tau_L}\right)$$

The normalized propagation delay of the three, cascaded amplifier stages can be given by

$$t_{p1}^{'} = \ln\left(\frac{3}{1 - \frac{v_{oa}}{A_v^3 v_{in}}}\right)$$

The normalized propagation delay of the latch can be given by

$$t_{p2}^{'} = \ln\left(\frac{V_{OH} - V_{OL}}{2v_{oa}}\right)$$

When $v_{in} = 0.05\left(V_{OH} - V_{OL}\right)$, and $v_{oa} = 0.1\left(V_{OH} - V_{OL}\right)$, the total normalized propagation delay is

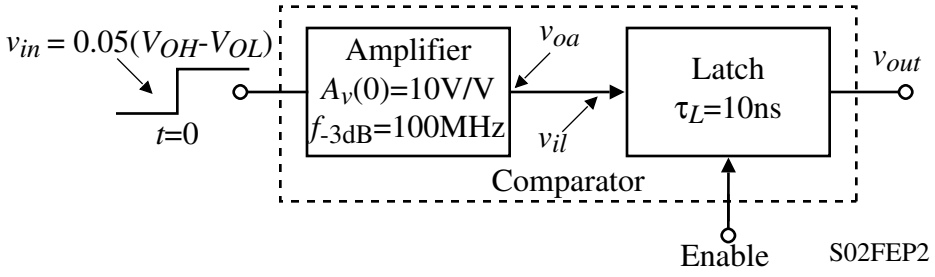
$$t_p^{'} = t_{p1}^{'} + t_{p2}^{'} = 1.115 + 1.609 = 2.724$$

When $v_{in} = 0.05\left(V_{OH} - V_{OL}\right)$, and $v_{oa} = 0.2\left(V_{OH} - V_{OL}\right)$, the total normalized propagation delay is

$$\boxed{t_p^{'} = t_{p1}^{'} + t_{p2}^{'} = 1.131 + 0.916 = 2.047}$$

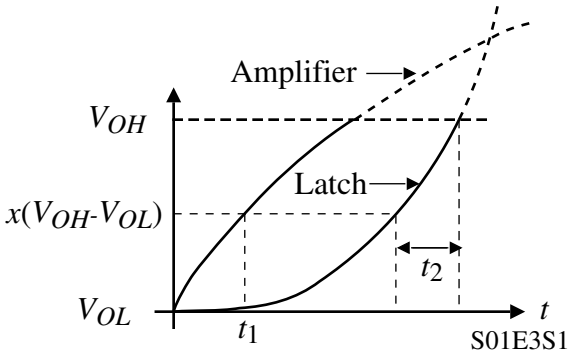
Problem 8.6-07

A comparator consists of an amplifier cascaded with a latch as shown in Figure P8.6-7. The amplifier has a voltage gain of 10 V/V and f_{-3dB} = 100 MHz and the latch has a time constant of 10 ns. The maximum and minimum voltage swings of the amplifier and latch are V_{OH} and V_{OL}. When should the latch be enabled after the application of a step input to the amplifier of $0.05(V_{OH} - V_{OL})$ to get minimum overall propagation time delay? What is the value of the minimum propagation time delay? It may be useful to recall that the propagation time delay of the latch is given as $t_p = \tau_L \ln\left(\frac{V_{OH} - V_{OL}}{2v_{il}}\right)$ where v_{il} is the latch input (ΔV_i of the text).



Solution

The solution is based on the figure shown.



We note that,

$$v_{oa}(t) = 10[1-e^{-\omega_{-3dB}t}]0.05(V_{OH}-V_{OL}).$$

If we define the input voltage to the latch as,

$$v_{il} = x\cdot(V_{OH}-V_{OL})$$

then we can solve for t_1 and t_2 as follows:

$$x\cdot(V_{OH}-V_{OL}) = 10[1-e^{-\omega_{-3dB}t_1}]0.05(V_{OH}-V_{OL}) \rightarrow x = 0.5[1-e^{-\omega_{-3dB}t_1}]$$

This gives,

$$t_1 = \frac{1}{\omega_{-3dB}} ln\left(\frac{1}{1-2x}\right)$$

From the propagation time delay of the latch we get,

$$t_2 = \tau_L ln\left(\frac{V_{OH}-V_{OL}}{2v_{il}}\right) = \tau_L ln\left(\frac{1}{2x}\right)$$

$$\therefore \quad t_p = t_1 + t_2 = \frac{1}{\omega_{-3dB}} ln\left(\frac{1}{1-2x}\right) + \tau_L ln\left(\frac{1}{2x}\right) \rightarrow \frac{dt_p}{dx} = 0 \text{ gives } x = \frac{\pi}{1+2\pi} = 0.4313$$

$$t_1 = \frac{10ns}{2\pi} ln\,(1+2\pi) = 1.592ns\cdot 1.9856 = \underline{\underline{3.16ns}} \text{ and } t_2 = 10ns\, ln\left(\frac{1+2\pi}{2\pi}\right) = 1.477ns$$

$$\therefore \quad t_p = t_1 + t_2 = 3.16ns + 1.477ns = \underline{\underline{4.637ns}}$$