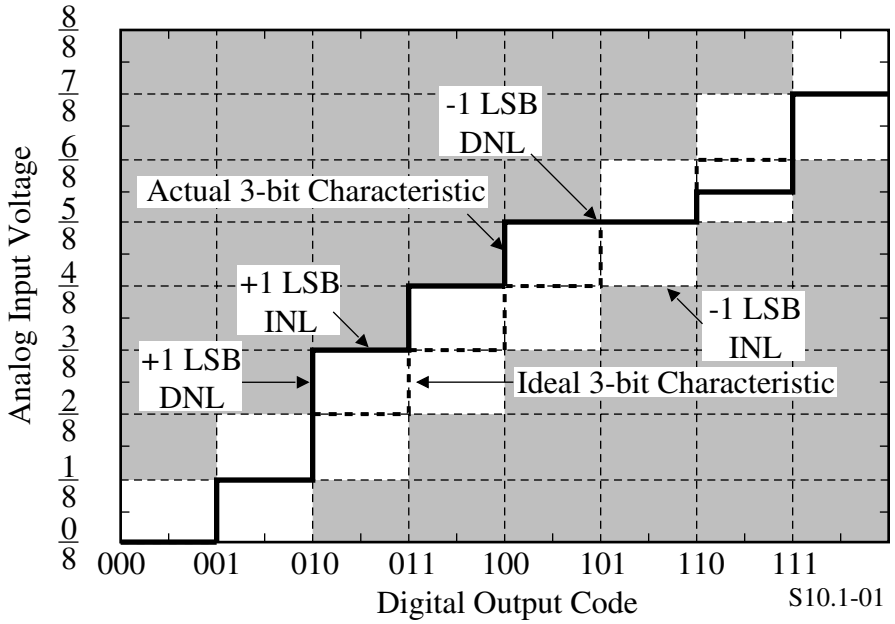
CHAPTER 10 – HOMEWORK SOLUTIONS

Problem 10.1-01

Plot the analog output versus the digital word input for a three-bit D/A converter that has ±1 LSB *DNL* and ±1 LSB *INL*. Assume an arbitrary analog full-scale value.

Solution

Below is a characteristic of a 3-bit DAC. The shaded area is not permitted in order to maintain ±1 LSB *INL*.

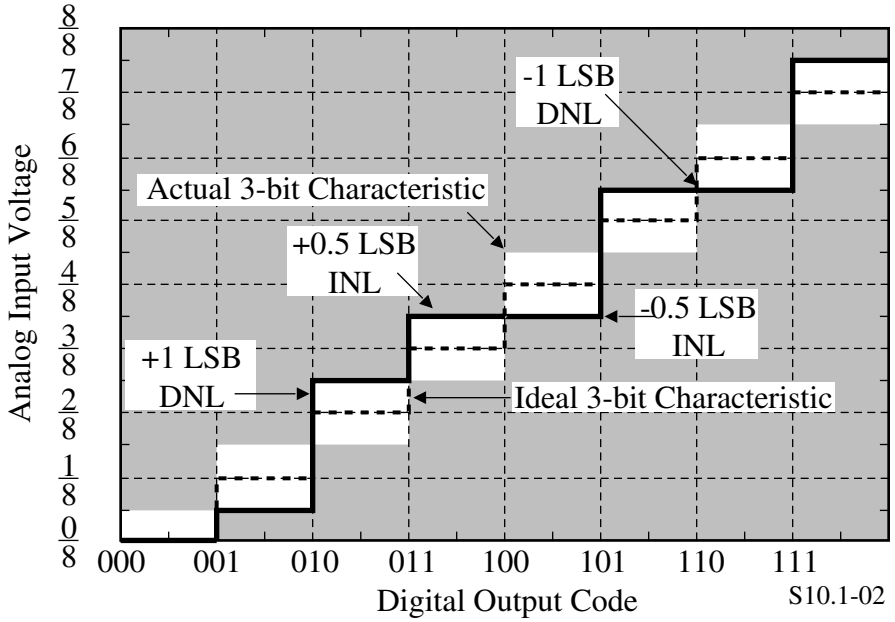


Problem 10.1-02

Repeat the above problem for ±1.5 LSB *DNL* and ±0.5 LSB integral linearity.

Solution

The shaded area is not permitted in order to maintain ±0.5 LSB *INL*. Note that the *DNL* cannot exceed ±1 LSB.

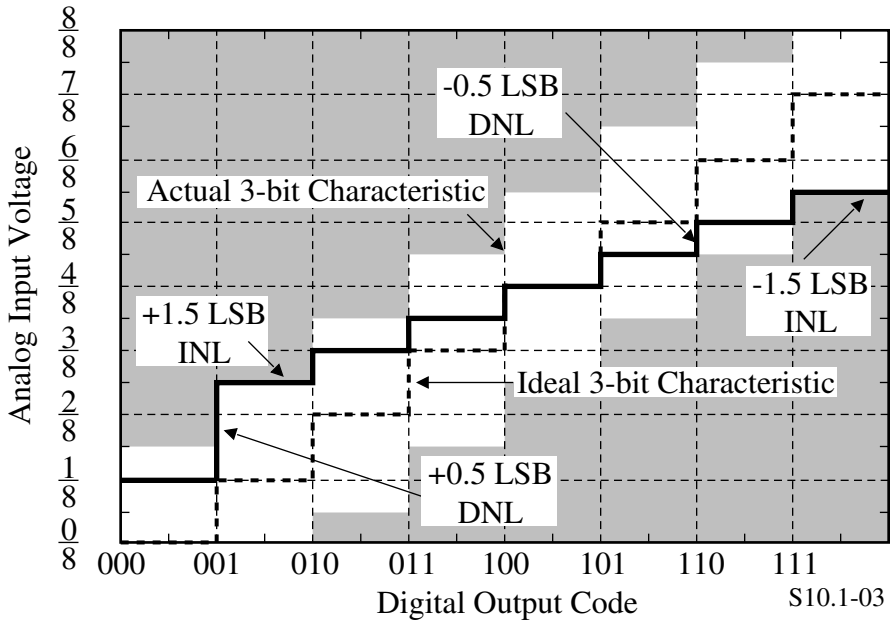


Problem 10.1-03

Repeat Prob. 1, for ±0.5 LSB differential linearity and ±1.5 LSB integral linearity.

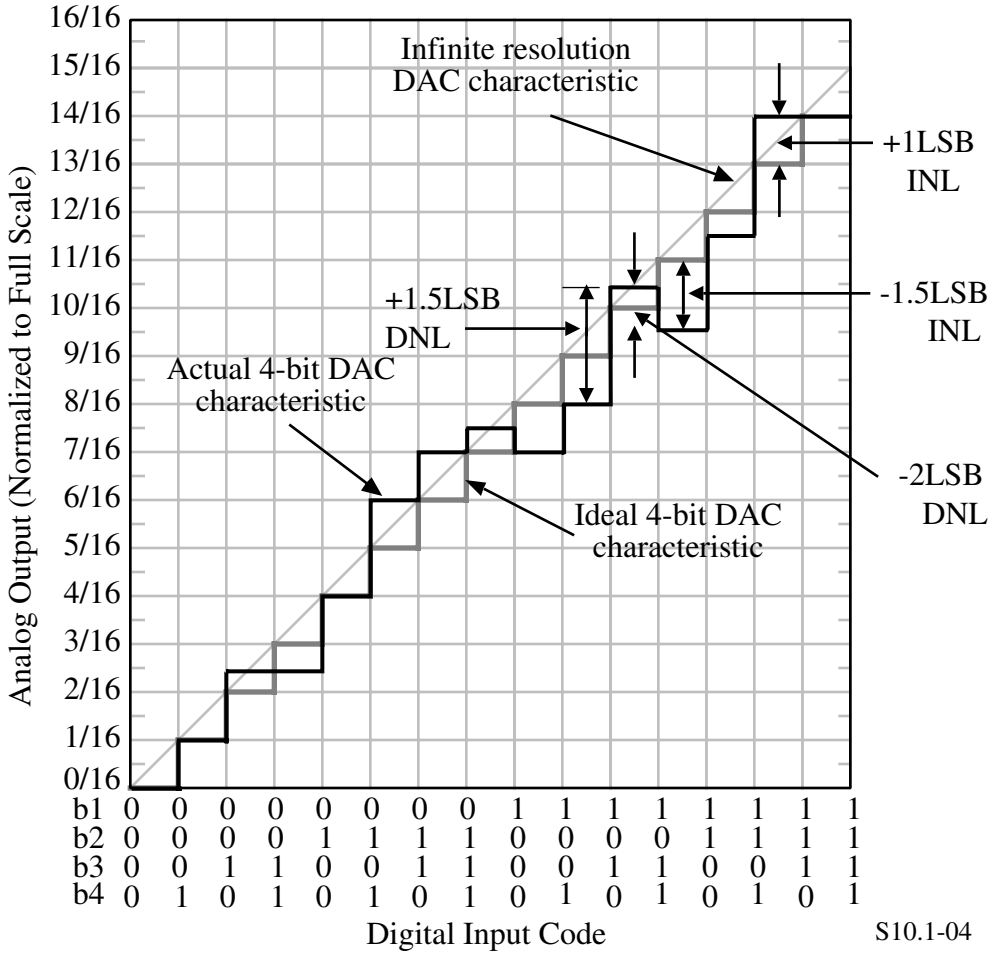
Solution

The shaded area is not permitted in order to maintain ±1.5 LSB *INL*.



Problem 10.1-04

The transfer characteristics of an ideal and actual 4-bit digital-analog converter are shown in Fig. P10.1-4. Find the ±INL and ±DNL in terms of LSBs. Is the converter monotonic or not?



Solution

INL: +1LSB, -2.5LSB, DNL: +1.5LSB, -2LSB, the converter is not monotonic.

Problem 10.1-05

A 1V peak-to-peak sinusoidal signal is applied to an ideal 10 bit DAC which has a V_{REF} of 5V. Find the SNR of the digitized analog output signal.).

Solution

A 1V peak sinusoideal signal is applied to an ideal 10 bit DAC which has a V_{REF} of 5V. Find the SNR of the digitized analog output signal.

Solution

The SNR_{max} = 6.02dB/bit x 10bits + 1.76dB = 61.96dB

The maximum output signal is 2.5V peak. Therefore, the 1V peak signal is 7.96dB smaller to give a *SNR* of the digitized analog output as 61.96-7.96 = 54dB

$\therefore$ $\boxed{SNR = 54\text{dB}}$

Problem 10.1-06

How much noise voltage in rms volts can a 1V reference voltage have and not cause errors in a 14-bit D/A converter? What must be the fractional temperature coefficient (ppm/°C) for the reference voltage of this D/A converter over the temperature range of 0°C to 100°C?

Solution

The rms equivalent of a 1V reference voltage is $\frac{1}{2\sqrt{2}}$V. Multiplying by $\frac{1}{2^{14}}$ gives

$$\text{Rms noise} = \frac{1}{2\sqrt{2}\cdot 2^{14}} = 21.6\mu\text{V(rms)} \rightarrow \boxed{\text{Rms noise} = 21.6\mu\text{V}}$$

To be within ±0.5*LSB*, the voltage change must be less than or equal to 2^{-15}.

$$\therefore \text{ ppm/C°} = \frac{\frac{\Delta V}{V}}{\Delta T} = \frac{\frac{2^{-15}}{1}}{100\text{C°}} = \frac{1}{2\cdot 16{,}384\cdot 100} = 0.3052\text{pppm/C°} \rightarrow \boxed{0.3052\text{ppm/C°}}$$

Problem 10.1-07

If the quantization level of an analog-to-digital converter is Δ, prove that the rms quantization noise is given as $\Delta/\sqrt{12}$.

Solution

Assume the quantizer signal appears as follows.

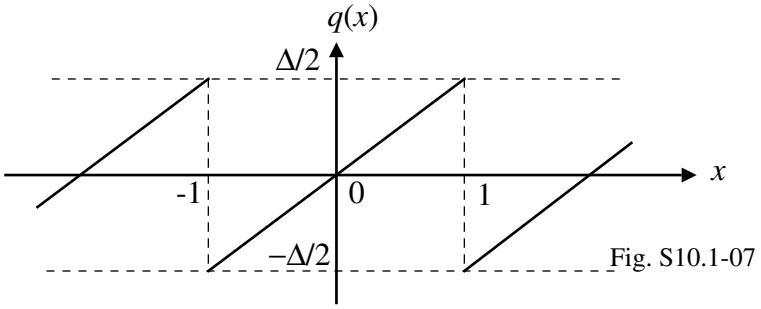


Fig. S10.1-07

The rms value of $q(x)$ is $\sqrt{\frac{1}{T}\int_0^T q^2(x)dx}$ where $q(x) = 0.5\Delta x$ and $T = 2$.

$$\therefore \text{ rms value of } q(x) = \sqrt{\frac{1}{2}\int_{-1}^{1}\frac{\Delta^2}{4}x^2dx} = \sqrt{\frac{\Delta^2}{8}\left.\frac{x^3}{3}\right|_{-1}^{1}} = \sqrt{\frac{\Delta^2}{8}\left(\frac{1}{3}+\frac{1}{3}\right)} = \frac{\Delta}{\sqrt{12}}$$

$$\text{rms value of } q(x) = \underline{\underline{\Delta/\sqrt{12}}}$$

Problem 10.2-01

Find I_o in terms of I_1, I_2, I_3, and I_4 for the circuit shown.

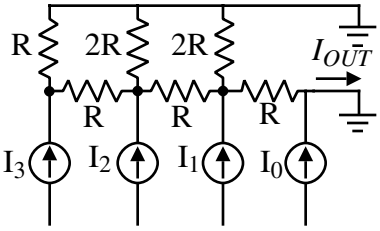


Figure P10.2-1

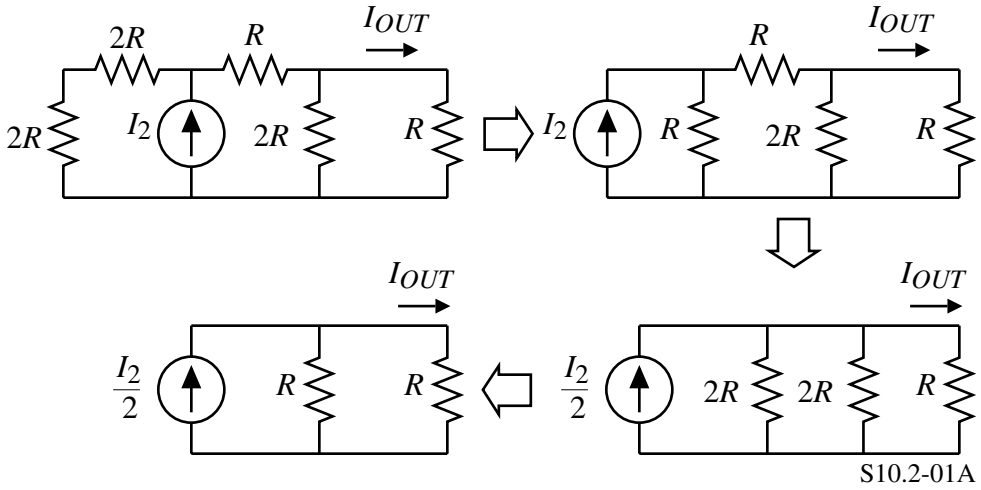
Solution

$$\boxed{I_{OUT} = I_0}$$

I_1 sees R to the right and R to the left so that $\boxed{I_{OUT} = \frac{I_1}{2}}$

.

I_2 requires the use of Norton's theorem to see the results.



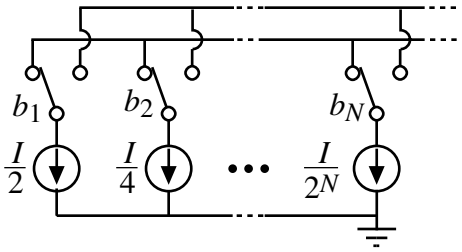
S10.2-01A

$\therefore$ $\boxed{I_{OUT} = \frac{I_2}{4}}$

Repeating the above process for I_8 will give $I_{OUT} = \boxed{I_{OUT} = \frac{I_3}{8}}$

Problem 10.2-02

A digital-analog converter uses the binary weighted current sinks shown. b_1 is the MSB and b_N is the LSB.



a.) For each individual current sink, find the tolerance in ±percent necessary to keep INL less than ±0.5LSB if $N = 4$ assuming all other bits are ideal.

b.) Considering the influence of all current sinks, what is the worst case tolerances in ±percent for each sink?

Solution

a.) An LSB $= \frac{\mathrm{I}}{2^N}$, therefore each sink must have the accuracy of ±0.5 LSB $= \frac{\pm \mathrm{I}}{2^{N+1}} = \frac{I}{32}$.

I/2: $\frac{I}{2} \pm \frac{\mathrm{I}}{2^{N+1}} = \frac{I}{2} \pm \frac{I}{32} = \frac{I}{2}\left(1 \pm \frac{1}{16}\right) \Rightarrow$

$$\text{Tolerance of } \frac{I}{2} = \frac{\pm\frac{1}{16}}{1} \text{x} 100\% = \frac{\pm 100}{16}\% = \pm 6.25\%$$

I/4: $\frac{I}{4} \pm \frac{I}{32} = \frac{I}{4}\left(1 \pm \frac{1}{8}\right) \Rightarrow$ $\text{Tolerance of } \frac{I}{4} = \frac{\pm\frac{1}{8}}{1} \text{x} 100\% = \frac{\pm 100}{8}\% = \pm 12.5\%$

Similarly, the tolerance of $I/8$ and $I/16$ are ±25% and ±50%, respectively.

$$\text{The tolerance of the ith current sink} = \frac{2^{i-N}}{2} \text{x} 100\%$$

b.) In this case, assume that all errors add for a worst case approach. Let this error be x. Therefore we can write,

$$\left(\frac{I}{2} + x\right) + \left(\frac{I}{4} + x\right) + \left(\frac{I}{8} + x\right) + \left(\frac{I}{16} + x\right) \le \left(\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}\right) + \frac{I}{32}$$

or

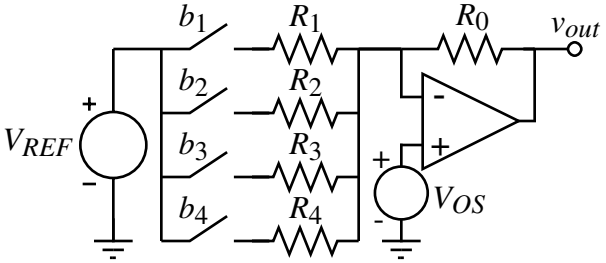
$$\left(\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}\right) + 4x \le \left(\frac{I}{2} + \frac{I}{4} + \frac{I}{8} + \frac{I}{16}\right) + \frac{I}{32} \Rightarrow x = \frac{I}{4 \cdot 32} = \frac{I}{128}$$

Thus the tolerances of part a.) are all decreased by a factor of 4 to give ±1.5625%, ±3.125%, ±6.25%, and ±12.5% for $I/2$, $I/4$, $I/8$, and $I/16$, respectively.

$$\frac{I}{2} \Rightarrow \pm 1.5625\%, \frac{I}{4} \Rightarrow \pm 3.125\%, \frac{I}{8} \Rightarrow \pm 6.25\% \text{ and } \frac{I}{16} \Rightarrow \pm 12.5\%$$

$$\text{The tolerance of the ith current sink} = \frac{2^{i-N}}{2N} \text{x} 100\%$$

Problem 10.2-03



A 4-bit, binary weighted, voltage scaling digital-to-analog converter is shown. (a.) If R_0 = 7R/8, $R_1 = 2R$, $R_2 = 4R$, $R_3 = 8R$, $R_4 = 16R$, and V_{OS} = 0V, sketch the digital-analog transfer curve on the plot on the next page. (b.) If $R_0 = R$, $R_1 = 2R$, $R_2 = 4R$, $R_3 = 8R$, $R_4 = 16R$, and $V_{OS} = (1/15)V_{REF}$, sketch the digital-analog transfer curve on the plot shown. (c.) If $R_0 = R$, $R_1 = 2R$, $R_2 = 16R/3$, $R_3 = 32R/5$, $R_4 = 16R$, and $V_{OS} = 0$V, sketch the digital-analog transfer curve on the previous transfer curve. For this case, what is the value of DNL and INL? Is this D/A converter monotonic or not?

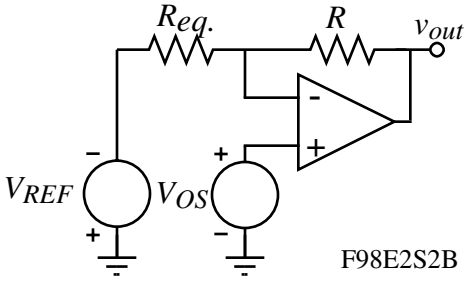
Solutions

(a.) $$v_{out} = R_0\left(\frac{b_1}{R_1} + \frac{b_2}{R_2} + \frac{b_3}{R_3} + \frac{b_4}{R_4}\right)V_{REF} = \frac{7}{8}\left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)V_{REF}$$

$$v_{out} = \left(\frac{7}{16} + \frac{7}{24} + \frac{7}{64} + \frac{7}{128}\right)V_{REF} = \frac{7}{8}\text{ x ideal characteristic}$$

(b.) The equivalent circuit is given as shown.

$$R_{eq} = \frac{R}{\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}}$$



$$v_{out} = \frac{R_0}{R_{eq.}}(V_{REF}+V_{OS}) + V_{OS}$$

$$v_{out} = \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)(V_{REF}-V_{OS}) + V_{OS}$$

$$v_{out} = \left(\frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16}\right)\left(\frac{16V_{REF}}{15}\right) + \frac{V_{REF}}{15}$$

$\therefore$ Gain error of 1/16 and offset of $V_{REF}/15$.

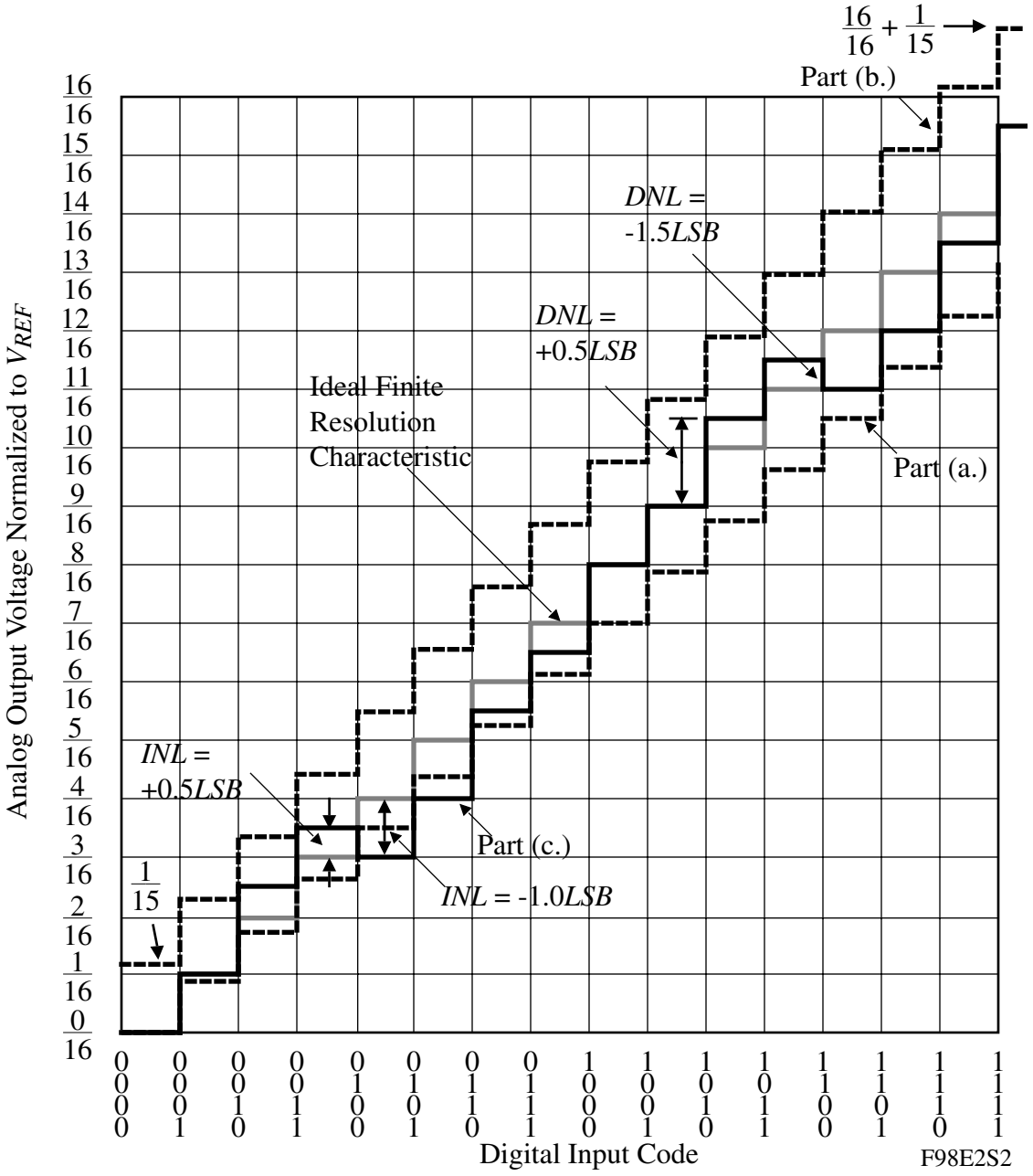
(c.) $$v_{out} = R_0\left(\frac{b_1}{R_1} + \frac{b_2}{R_2} + \frac{b_3}{R_3} + \frac{b_4}{R_4}\right)V_{REF} = \left(\frac{b_1}{2} + \frac{3b_2}{16} + \frac{5b_3}{32} + \frac{b_4}{16}\right)V_{REF}$$

$$= \left(\frac{16b_1}{32} + \frac{12b_2}{32} + \frac{5b_3}{32} + \frac{2b_4}{32}\right)V_{REF} \rightarrow \text{Used to generate the plot on the next page}$$

$\therefore$ $INL = +0.5LSB$ and $-1.0LSB$ $\quad DNL = +0.5LSB$ and $-1.5LSB$

This DAC is not monotonic.

Problem 10.2-3 - Continued



Problem 10.2-04

A 4-bit digital-to-analog converter characteristic using the DAC of Fig. P10.2-3 is shown in Fig. P10.2-4. (a.) Find the *DNL* and the *INL* of this converter. (b.) What are the values of R_1 through R_4, that correspond to this input-output characteristic? Find these values in terms of R_0.

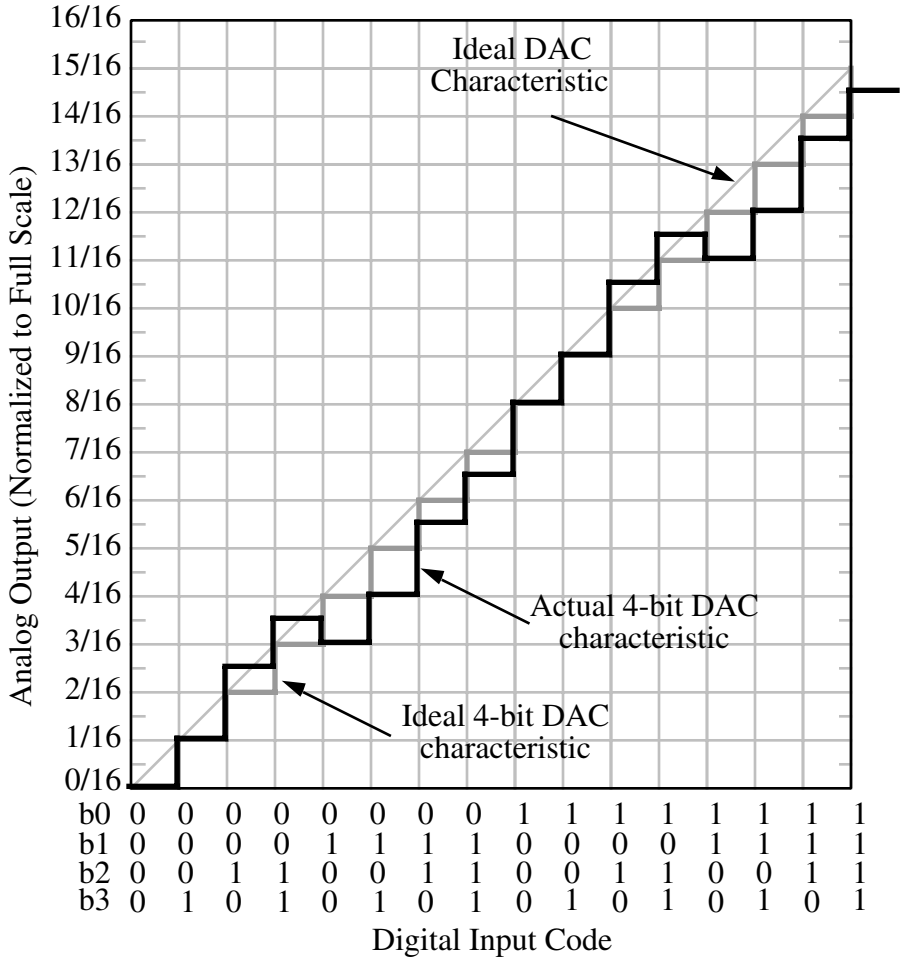


Figure P10.2-4

Solution

(a.) INL = +0.5LSB and –2.0 LSB, DNL = +0.5LSB and –1.5LSB.

(b.) Note that v_{OUT} can be written as,

$$v_{OUT} = -R_0\left[\frac{b_0}{R_1} + \frac{b_1}{R_2} + \frac{b_2}{R_3} + \frac{b_3}{R_4}\right] V_{REF}$$

For 0001, $|v_{OUT}| = \dfrac{V_{REF}}{16} \rightarrow R_4 = 16\,R_0$. For 0010, $|v_{OUT}| = \dfrac{5V_{REF}}{32} \rightarrow R_3 = \dfrac{32}{5} R_0$.

For 0100, $|v_{OUT}| = \dfrac{3V_{REF}}{16} \rightarrow R_2 = \dfrac{16}{3}\,R_0$. For 1000, $|v_{OUT}| = \dfrac{V_{REF}}{2} \rightarrow R_1 = 2\,R_0$

Problem 10.2-05

For the DAC of Fig. P10.2-3, design the values of R_1 through R_4 in terms of R_0 to achieve an ideal 4-bit DAC. What value of input offset voltage, V_{OS}, normalized to V_{REF} will cause an error? If the op amp has a differential voltage gain of

$$A_{vd}(s) = \frac{10^6}{s + 100}$$

at what frequency or rate of conversion will an error in conversion occur due to the frequency response of the op amp? Assume that the rate of application of digital words to be converted is equivalent to the application of a sinusoidal signal of equivalent frequency.

Solution

The values of the resistors are $R_1 = 2R_0$, $R_2 = 4R_0$, $R_3 = 8R_0$, and $R_4 = 16R_0$.
A model for the input offset voltage influence on the DAC is shown. The output voltage is,

$$v_{OUT} = -\frac{R}{R_{EQ.}} V_{REF} + \left(\frac{R + R_{EQ.}}{R_{EQ.}}\right) V_{OS}$$

We see that the largest influence of V_{OS} is when $R_{EQ.}$ is minimum which is $R_1 \| R_2 \| R_3 \| R_4 = (16/15)R$.

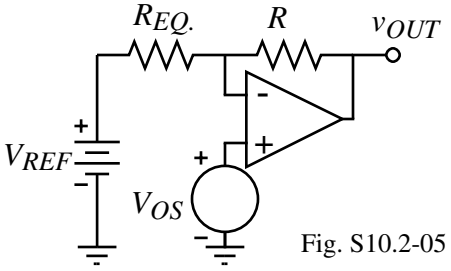


Fig. S10.2-05

$$\therefore \quad \left(1 + \frac{15}{16}\right) V_{OS} \le 0.5\text{LSB} = \frac{1}{32} V_{REF}$$

$$\frac{V_{OS}}{V_{REF}} \le \left(\frac{1}{32}\right)\left(\frac{16}{31}\right) = \frac{1}{62} = \underline{\underline{0.01613}}$$

For the maximum conversion rate, the worst case occurs when the loop gain is smallest. The loop gain is given as

$$LG = -\left(\frac{R_{EQ.}}{R + R_{EQ.}}\right) A_{vd}$$

Which is minimum when $R_{EQ.} = (16/15)R$. The ideal output normalized to V_{REF} is,

$$\frac{v_{OUT}(\text{ideal})}{V_{REF}} = -\left(\frac{R}{R_{EQ.}}\right) = -\frac{15}{16}$$

The actual output normalized to V_{REF} is,

$$\frac{v_{OUT}(\text{actual})}{V_{REF}} = \frac{-\dfrac{A_{vd}R}{R + R_{EQ.}}}{1 + \dfrac{A_{vd}R_{EQ.}}{R + R_{EQ.}}} = \frac{-\dfrac{15}{31}}{\dfrac{1}{A_{vd}} + \dfrac{16}{31}} = \frac{-\dfrac{15}{31}}{\dfrac{s}{10^6} + \dfrac{16}{31}}$$

where we have assumed that $\omega >> 100$ rads/sec which gives $A_{vd}(s) \approx 10^6/s$.

An error occurs when $\left|\dfrac{v_{OUT}(\text{actual})}{V_{REF}}\right| \ge \dfrac{15}{16} - \dfrac{1}{32} = \dfrac{29}{32}$ (Actual is always less than ideal)

$$\frac{\dfrac{15}{31}}{\sqrt{\left(\dfrac{\omega_{\max}}{10^6}\right)^2 + \left(\dfrac{16}{31}\right)^2}} \ge \frac{29}{32} \quad \rightarrow \quad \left(\frac{16}{31}\right)^2 + \left(\frac{\omega_{\max}}{10^6}\right)^2 \le \left(\frac{15}{31}\right)^2 \left(\frac{32}{29}\right)^2$$

$$\frac{\omega_{\max}}{10^6} \le \sqrt{\left(\frac{15}{31} \times \frac{32}{29}\right)^2 - \left(\frac{16}{31}\right)^2} = 0.1367$$

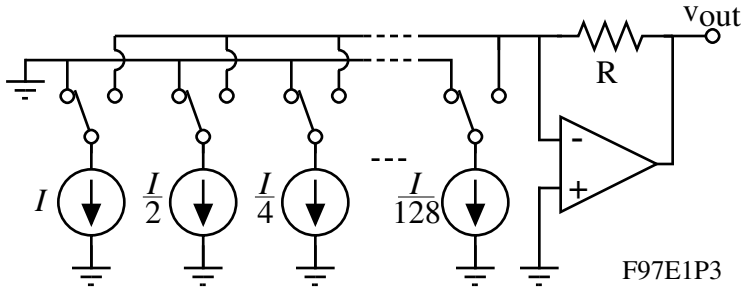
Problem 10.2-05- Continued

$\therefore \quad \omega_{max} \le 0.1367 \times 10^6$ rads/sec. $\quad \rightarrow \quad f_{max} \le \underline{21.76 \text{ kHz}}$

Note that 21.76 kHz is much greater than 15.9 Hz (100 rads/sec.) so that the approximation used for $A_{vd}(s)$ is valid.

Problem 10.2-06

An 8-bit current DAC is shown. Assume that the full scale range is 1V. (a.) Find the value of I if $R = 1\text{k}\Omega$. (b.) Assume that all aspects of the DAC are ideal except for the op amp. If the differential voltage gain of the op amp has a single pole frequency response with a dc gain of 10^5. Find the unity gainbandwidth, GB, in Hz that gives a worst case conversion time of 2μs. (c.) Again assume that all aspects of the DAC are ideal except for the op amp. The op amp is ideal except for a finite slew rate. Find the minimum slew rate, SR, in V/μs that gives a worst case conversion time of 2μs.



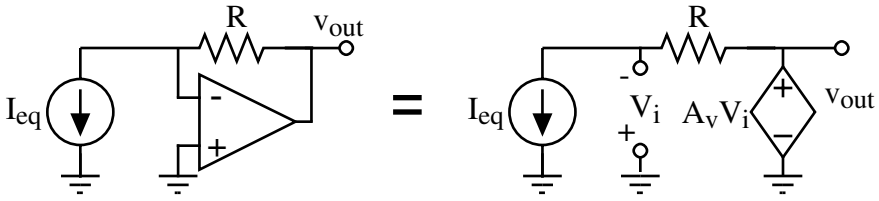
Solution

(a.) FSR = 2I·R = 1V $\Rightarrow$ I = 1V/2kΩ = 500μA $\quad \therefore \quad$ **I = 500μA**

(b.) Model for part b.

I_{eq} = all bits switched to the op amp input.

The worst case occurs when all bits are switched to the op amp.



$$\therefore \; V_{out} = A_v V_i = A_v[RI_{eq} - V_{out}] \Rightarrow V_{out}(1+A_v) = A_v RI_{eq} \Rightarrow V_{out} = \frac{RI_{eq}}{\frac{1}{A_v} + 1}$$

or $\quad V_{out}(s) = \dfrac{RI_{eq}}{\frac{s}{GB} + 1} \quad$ Assuming a step input gives $V_{out}(s) = \left(\dfrac{RI_{eq}}{\frac{s}{GB} + 1}\right)\dfrac{1}{s}$

$$\therefore \quad \mathcal{L}^{-1}[V_{out}(s)] = v_{out}(t) = RI_{eq}[1 - e^{-GB \cdot t}]\, \mu(t)$$

$\text{Error}(t) = RI_{eq} - v_{out}(t) \Rightarrow \text{Error}(T) = e^{-GB \cdot T} = 1/2^{8+1} = 1/512 \Rightarrow e^{GB \cdot T} = 512$

If T= 2μs, then GB is given as $GB = 0.5 \times 10^6 \ln(512) = 3.119 \times 10^6$ $\therefore$ **GB= 0.496MHz**

(c.) Slew Rate:

Want $\Delta V/\Delta T$ = 1V/2μs = 0.5V/μs assuming a $\Delta V \approx 1$V. $\therefore$ **SR = 0.5V/μs**

Problem 10.2-07

What is the necessary relative accuracy of resistor ratios in order for a voltage-scaling DAC to have a 8-bit resolution?

Solution

Since the voltage scaling DAC has very small DNL errors, let the 8-bit accuracy requirement be determined by the INL error.

$$INL = 2^{N-1}\frac{\Delta R}{R} \le 0.5 \qquad \rightarrow \qquad \frac{\Delta R}{R} \le \frac{1}{2}\,\frac{2}{2^N} = \frac{1}{2^N} = \frac{1}{256}$$

$$\therefore \qquad \boxed{\frac{\Delta R}{R} \le 0.39\%}$$

Problem 10.2-08

If the binary controlled switch b_1 of Fig. P10.2-3 is closed at t =0, find the time it takes the output to achieve its final stage ($-V_{REF}/2$) by assuming that this time is 4 times the time constant of this circuit. The differential voltage gain of the op amp is given as

$$A_{vd}(s) = \frac{10^6}{s + 10}.$$

Solution

The model show will be used for this solution.

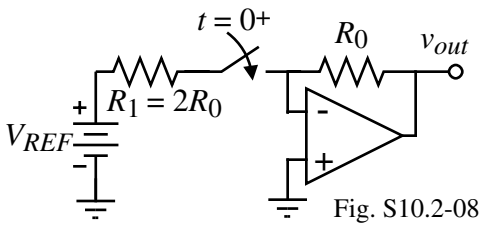


Fig. S10.2-08

The transfer function for this problem can be written as,

$$\frac{V_{out}(s)}{V_{in}(s)} = -\left(\frac{R_0}{R_1}\right)\frac{\dfrac{R_1 A_{vd}(s)}{R_1+R_0}}{1+\dfrac{R_1 A_{vd}(s)}{R_1+R_0}} = -0.5$$

$$\frac{1}{\dfrac{1.5}{A_{vd}(s)}+1} \approx -0.5\,\frac{1}{\dfrac{1.5s}{GB}+1} = -0.5\left(\frac{0.667\text{x}10^6}{s+0.667\text{x}10^6}\right)$$

For a step input of magnitude V_{REF}, we can write,

$$V_{out}(s) = -0.5\left(\frac{0.667\text{x}10^6}{s+0.667\text{x}10^6}\right)\frac{V_{REF}}{s} = -0.5\left[\frac{1}{s} - \frac{1}{s+0.667\text{x}10^6}\right]V_{REF}$$

The inverse Laplace transform gives,

$$v_{out}(t) = -0.5[1-e^{-0.667\text{x}10^6 t}]V_{REF}$$

The time constant of this circuit is $1/(0.667\text{x}10^6)$ = 1.5μs which means that it will take 6μs for the DAC to convert the switch change to the output voltage.

∴ Time for conversion = 6μs.

Problem 10.2-09

What is the necessary relative accuracy of capacitor ratios in order for a charge-scaling DAC to have 11-bit resolution?

Solution

Perfect *DNL* will be impossible to achieve so let us use *INL* to answer the question and see what the *DNL* is based on the *INL*.

$$INL = 2^{N-1}\frac{\Delta C}{C} \le 0.5 \qquad \rightarrow \qquad \frac{\Delta C}{C} \le \frac{1}{2}\frac{2}{2^N} = \frac{1}{2^N} = \frac{1}{2048}$$

$$\therefore \quad \boxed{\frac{\Delta C}{C} \le 0.0488\%} \qquad \text{The corresponding } DNL = (2^N-1)\frac{\Delta C}{C} \approx \pm 1\text{LSB}$$

Problem 10.2-10

For the charge scaling DAC of Fig. 10.2-10, investigate the influence of a load capacitor, C_L, connected in parallel with the terminating capacitor. (a.) Find an expression for v_{OUT} as a function of C, C_L, the digital bits, b_i, and V_{REF}. (b.) What kind of static error does C_L introduce? (c.) What is the largest value of C_L/C possible before an error is introduced in this DAC?

Solution

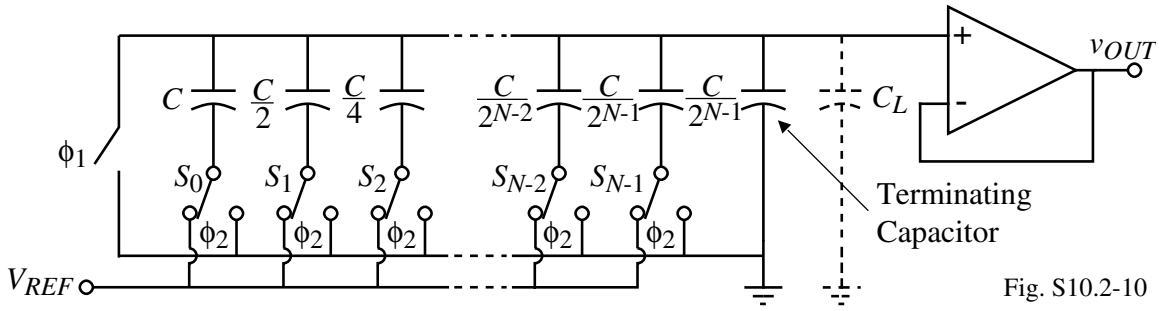


Fig. S10.2-10

(a.) Charge conservation gives,

$$C_{Total}v_{OUT} = \left(b_0 C + b_1\frac{C}{2} + b_2\frac{C}{4} + \cdots + b_{N-2}\frac{C}{2^{N-2}} + b_{N-1}\frac{C}{2^{N-1}}\right)V_{REF}$$

where $C_{Total} = 2C + C_L$.

$$v_{OUT} = \left(\frac{C}{2C + C_L}\right)\left(b_0 + \frac{b_1}{2} + \frac{b_2}{4} + \cdots + \frac{b_{N-2}}{2^{N-2}} + \frac{b_{N-1}}{2^{N-1}}\right)V_{REF}$$

$$\therefore \quad v_{OUT} = \left(\frac{1}{1 + \frac{C_L}{2C}}\right)\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N}\right)V_{REF}$$

(b.) If $C_L << 2C$, then $v_{OUT} \approx \left(1 - \frac{C_L}{2C}\right)\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N}\right)V_{REF}$

which introduces a gain error.

(c.) From the previous result, the error term can be written as,

$$\frac{C_L}{2C}\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N}\right)V_{REF} \le \frac{1}{2}\frac{V_{REF}}{2^N} = 0.5 \text{ LSB}$$

$$\frac{C_L}{C} \le \frac{1}{2^N\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \cdots + \frac{b_{N-2}}{2^{N-1}} + \frac{b_{N-1}}{2^N}\right)} \approx \frac{1}{2^N}$$ when all bits are 1 and $N > 1$.

Problem 10.2-11

Express the output of the D/A converter shown in Fig. P10.2-11 during the ϕ_2 period as a function of the digital bits, b_i, the capacitors, and the reference voltage, V_{REF}. If the op amp has an offset of V_{OS}, how is this expression for the output changed? What kind of error will the op amp offset cause?

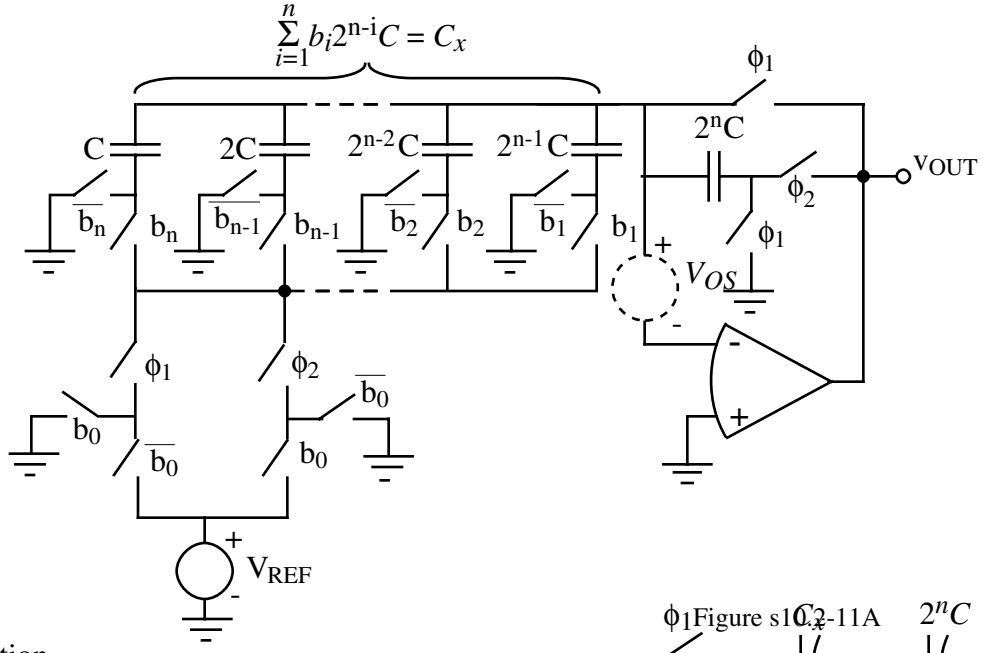


Figure s10.2-11A

Solution

$V_{OS} = 0$:

$b_0 = 1$: $\quad v_{OUT} = -\dfrac{C_x}{2^n C} V_{REF}$

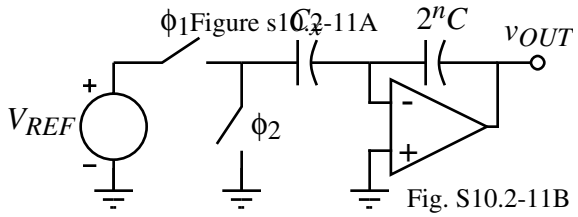


Fig. S10.2-11B

$$v_{OUT} = -\left(\frac{\sum_{i=1}^{n} b_i 2^n 2^{-i} C}{2^n C}\right) V_{REF} \quad \rightarrow \quad \boxed{v_{OUT} = -\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right) V_{REF}}$$

($b_0 = 1$)

$b_0 = 0$: Reverse ϕ_1 and ϕ_2 to get,

$$\boxed{v_{OUT} = +\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right) V_{REF}} \quad (b_0 = 0)$$

Problem 10.2-11 – Continued

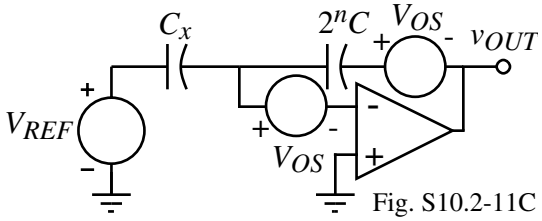


Fig. S10.2-11C

$V_{OS} \neq 0$:

At ϕ_2 we have,

From this circuit, we can write that,

$$C_x(V_{REF} - V_{OS}) = 2^nC(V_{OS} - V_{OS} - v_{OUT})$$

or

$$v_{OUT} = -\frac{C_x}{2^nC}(V_{REF} - V_{OS})$$

$$\therefore \quad \boxed{v_{OUT} = -\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right)(V_{REF} - V_{OS})} \qquad (b_0 = 1)$$

and

$$\boxed{v_{OUT} = +\left(\sum_{n}^{i=1} \frac{b_i}{2^i}\right)(V_{REF} - V_{OS})} \qquad (b_0 = 0)$$

V_{OS} causes a gain error.

Problem 10.2-12

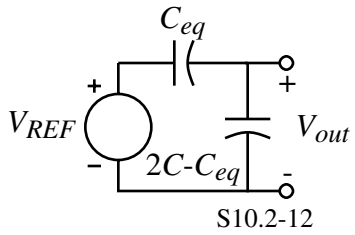
Develop the equivalent circuit of Fig. 10.2-11 from Fig. 10.2-10.

Solution

For each individual capacitor connected only to V_{REF} we can write,

$$V_{out} = V_{REF}\ \frac{C}{2C},\ V_{out} = V_{REF}\ \frac{C}{4C},\ V_{out} = V_{REF}\ \frac{C}{8C},\ \ldots..$$

Note that the numerator consists only of the capacitances connected to V_{REF}. If these capacitors sum up to C_{eq}. then the remaining capacitors must be $2C$ - C_{eq}. Therefore, we have,



S10.2-12

Problem 10.2-13

If the tolerance of the capacitors in the 8-bit, binary-weighted array shown in Fig. P10.2-13 is ±0.5%, what would be the worst case *DNL* in units of *LSBs* and at what transition does it occur?

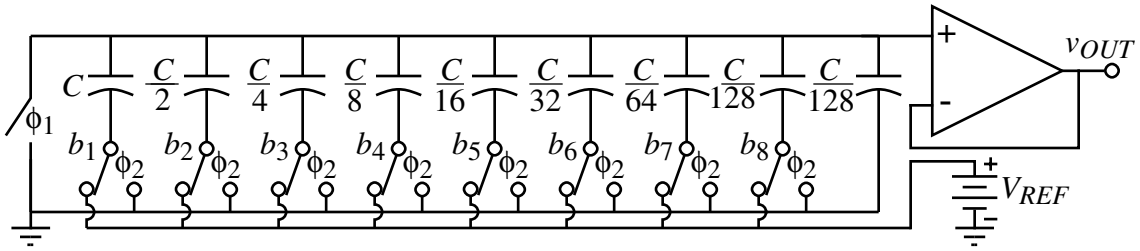


Figure P10.2-13

Solution

The worst case *DNL* occurs at the transition form 01111111 to 10000000.

+*DNL*:

Ideally, $v_{OUT} = \dfrac{C_{eq}}{2C\text{-}C_{eq} + C_{eq}} V_{REF}$. The worst case is found by assuming that all of the C_{eq} capacitors are maximu and the $2C\text{-}C_{eq}$ capacitors are minimum. However, for the above transition, the maximum, worst case positive step can be written as

$$\text{Max. step} = v_{OUT}(10000000) - v_{OUT}(01111111) = V_{REF}\left[\frac{1.005}{2} - \frac{0.995}{2}\left(1 - \frac{1}{128}\right)\right]$$

$$= \frac{V_{REF}}{2}\left[1.005 - 0.995\left(1 - \frac{1}{128}\right)\right] = \frac{V_{REF}}{2}[1.005 - 0.995(0.9922)]V_{REF}$$

$$= 0.008887V_{REF}$$

$$\text{An LSB} = V_{REF}/256 = 0.003906V_{REF}$$

$$\therefore \quad \boxed{+\text{DNL} = \frac{0.008887}{0.003906} - 1 = 2.275 - 1 = 1.275 \text{ LSB}}$$

-*DNL*:

For this case, let the C_{eq} capacitors be minimum and the $2C\text{-}C_{eq}$ capacitors be maximum. Following the same development as above gives,

$$\text{Min. step} = v_{OUT}(10000000) - v_{OUT}(01111111) = V_{REF}\left[\frac{0.995}{2} - \frac{1.005}{2}\left(1 - \frac{1}{128}\right)\right]$$

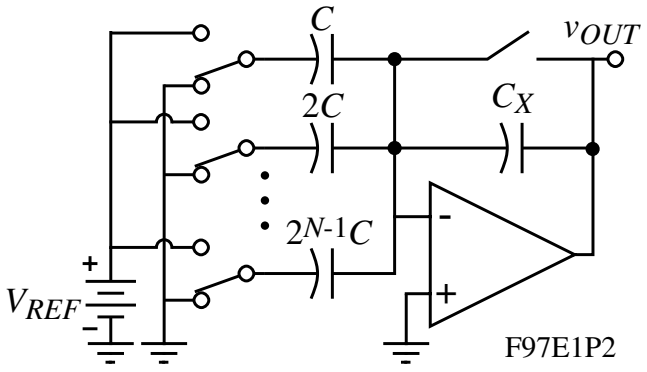
$$= \frac{V_{REF}}{2}\left[0.995 - 1.005\left(1 - \frac{1}{128}\right)\right] = \frac{V_{REF}}{2}[0.995 - 1.005(0.9922)]V_{REF}$$

$$= -0.001074V_{REF}$$

$$\therefore \quad \boxed{-\text{DNL} = \frac{-0.001074}{0.003906} - 1 = -0.2750 - 1 = -1.275 \text{ LSB}}$$

Problem 10.2-14

A binary weighted DAC using a charge amplifier is shown. At the beginning of the digital to analog conversion, all capacitors are discharged. If a bit is 1, the capacitor is connected to V_{REF} and if the bit is 0 the capacitor is connected to ground.



F97E1P2

a.) Design C_X to get

$$v_{OUT} = \left(\frac{b_1}{2} + \frac{b_2}{4} + \cdots + \frac{b_N}{2^N} \right) V_{REF} .$$

b.) Identify the switches by b_i where $i = 1$ is the MSB and $i = N$ is the LSB.

c.) Find the maximum component spread (largest value/smallest value) for the capacitors.

d.) Is this DAC fast or slow? Why?

e.) Can this DAC be nonmonotonic?

f.) If the relative accuracy of the capacitors are 0.2% (regardless of capacitor sizes) what is the maximum value of N for ideal operation?

Solution

a.) Solving for v_{OUT} gives

$$v_{OUT} = \left(\frac{C}{C_X} + \frac{2C}{C_X} + \cdots + \frac{2^{N-1}C}{C_X} \right) V_{REF} , \text{ therefore } \boxed{C_X = 2^N C} \text{ which gives}$$

$$v_{OUT} = \left(\frac{1}{2^N} + \frac{1}{2^{N-1}} + \cdots + \frac{1}{2} \right) V_{\mathrm{REF}}$$

b.) See schematic for switch identification.

c.) The maximum component spread is C_X/C which is $\boxed{\text{Max. component spread} = 2^N}$

d.) This DAC should be fast because there are no floating nodes.

e.) Yes, the DAC can be nonmonotonic.

f.) Let C_{eq} be all capacitors connected to V_{REF}. $\therefore \frac{v_{out}}{V_{REF}} = - \frac{C_{eq}}{C_x}$.

For the worst case, let C_{eq} be $C_{eq} + \Delta C_{eq}$ and C_x be $C_x - \Delta C_x$ which gives

$$\frac{v_{out}'}{V_{REF}} = - \frac{C_{eq}+\Delta C_{eq}}{C_x - \Delta C_x} = - \frac{C_{eq}}{C_x} \left(\frac{1+\Delta C_{eq}/C_{eq}}{1-\Delta C_x/C_x} \right) = - \frac{C_{eq}}{C_x} \left(\frac{1+0.002}{1-0.002} \right) = - \frac{C_{eq}}{C_x} \left(\frac{501}{499} \right)$$

$$\therefore \left| \frac{v_{out}}{V_{REF}} - \frac{v_{out}'}{V_{REF}} \right| = \left| - \frac{C_{eq}}{C_x} + \left(\frac{501}{499} \right) \frac{C_{eq}}{C_x} \right| = \frac{2}{499} \frac{C_{eq}}{C_x} \le \frac{1}{2^{N+1}}$$

The largest value of C_{eq}/C_x is $(2^N-1)/2^N$. $\therefore \frac{2}{499} \le \frac{2^N}{(2^N-1)(2^N+1)} = \frac{1}{2^N} \Rightarrow \boxed{N = 7}$

(Note that N is almost equal to 8.)

Problem 10.2-15

A binary weighted DAC using The circuit shown is an equivalent for the operation of a DAC. The op amp differential voltage gain, $A_{vd}(s)$ is modeled as

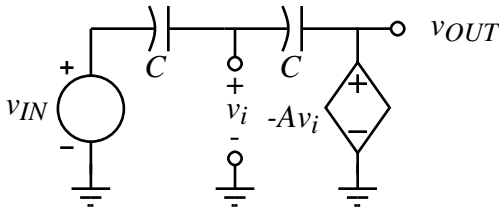
$$A_{vd}(s) = \frac{A_{vd}(0)\,\omega_a}{s + \omega_a} = \frac{GB}{s + \omega_a}.$$

a.) If ω_a goes to infinity so that $A_{vd}(s) \approx A_{vd}(0)$, what is the minimum value of $A_{vd}(0)$ that will cause a ±0.5 LSB error for an 8-bit DAC?

b.) If $A_{vd}(0)$ is larger than the value found in a.), what is the minimum conversion time for an 8-bit DAC which gives a ±0.5 LSB error if GB = 1Mhz?

Solution

a.) Model for the circuit:



$$v_i = \left(\frac{C}{C+C}\right)v_{REF} + \left(\frac{C}{C+C}\right)v_{OUT}$$

and

$$v_{OUT} = -Av_i$$

$$\therefore\ v_{OUT} = \frac{-A}{2}v_{OUT} - \frac{A}{2}v_{REF} \quad \Rightarrow \quad \frac{v_{OUT}}{v_{REF}} = \frac{\frac{-A}{2}}{1 + \frac{A}{2}}$$

Setting the actual gain to -1±0.5LSB gives

$$\frac{-0.5A}{1+0.5A} = -\left(1 - \frac{1}{2}\left(\frac{1}{256}\right)\right) = \frac{-511}{512} \quad \Rightarrow \quad -\frac{512A}{2} = -511 - \frac{511A}{2} \quad \Rightarrow \quad \frac{A}{2} = 511 \quad \Rightarrow$$

$$\boxed{A = 1022}$$

b.) If $A_{vd}(s) \approx -GB/s$, then the s-domain transfer function can be written as

$$\frac{V_{out}(s)}{V_{REF}} = \frac{-GB/2}{s + GB/2} = \frac{-\omega_H}{s + \omega_H} \quad \Rightarrow \quad \omega_H = \frac{2\pi\cdot 10^6}{2} = \pi\cdot 10^6$$

The time domain output can be written as

$$v_{out}(t) = -1[1 - e^{-\omega_H t}]V_{REF}$$

Setting $v_{out}(t)$ = -1±0.5LSB and solving for the time, T, at which this occurs gives

$$-1 + e^{-\omega_H T} = -1 + \frac{1}{512} \ \Rightarrow\ e^{\omega HT} = 512 \ \Rightarrow\ \omega_H T = ln(512) \ \Rightarrow\ T = \frac{6.283}{3.1416\text{x}10^6}$$

or

$$\boxed{T = 1.9857\mu s}$$

Problem 10.2-16

A charge-scaling DAC is shown in Fig. P10.2-16 that uses a *C*-2*C* ladder. All capacitors are discharged during the ϕ_1 phase. (a.) What value of C_F is required to make this DAC work correctly? (b.) Write an expression for v_{OUT} during ϕ_2 in terms of the bits, b_i, and the reference voltage, V_{REF}. (c.) Discuss at least two advantages and two disadvantages of this DAC compared to other types of DACs.

Solution

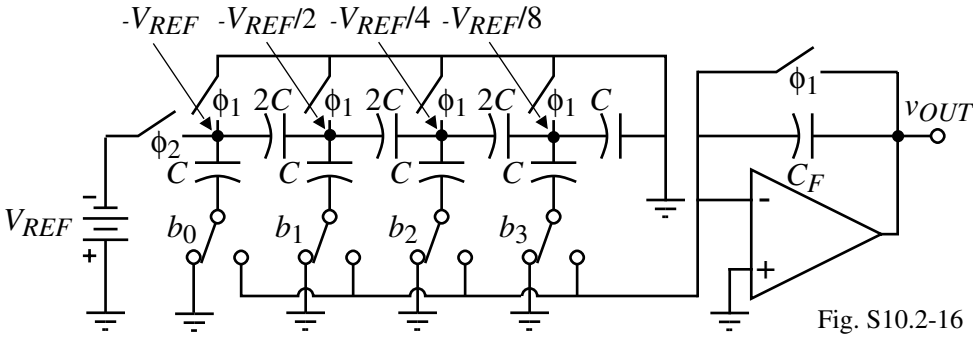


Fig. S10.2-16

(a.) $\boxed{C_F = 2C}$

(b.) $$v_{OUT} = \left(\frac{b_0}{2}\right)V_{REF} + \left(\frac{b_1}{2}\right)\frac{V_{REF}}{2} + \left(\frac{b_2}{2}\right)\frac{V_{REF}}{4} + \left(\frac{b_3}{2}\right)\frac{V_{REF}}{8}$$

$$\boxed{v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right)V_{REF}}$$

(c.) Advantages:

1.) Smaller area than binary-weighted DAC.

2.) Better accuracy because the components differ by only 2:1.

3.) Autozeros the offset of the op amp.

Disadvantages:

1.) Has floating nodes and is sensitive to parasitics.

2.) Parasitic capacitances at the floating nodes will deteriorate the accuracy.

3.) Can be nonmonotonic.

4.) Requires a two-phase, non-overlapping clock.

Problem 10.3-01

The DAC of Fig. 10.3-1 has $m = 2$ and $k = 2$. If the divisor has an incorrect value of 2, express the $\pm INL$ and the $\pm DNL$ in terms of *LSBs* and determine whether or not the DAC is monotonic. Repeat if the divisor is 6.

Solution

The general form for the output of this DAC is,

$$\frac{v_{OUT}}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{2k} + \frac{b_3}{4k}$$

$k = 2$:

$$\frac{v_{OUT}}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{4} + \frac{b_3}{8}$$

The result is:

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.12500	0.00000	1.00000	0.00000	1.00000
0	0	1	0	0.12500	0.25000	0.00000	1.00000	0.00000	2.00000
0	0	1	1	0.18750	0.37500	0.00000	1.00000	0.00000	3.00000
0	1	0	0	0.25000	0.25000	0.00000	-3.00000	0.00000	0.00000
0	1	0	1	0.31250	0.37500	0.00000	1.00000	0.00000	1.00000
0	1	1	0	0.37500	0.50000	0.00000	1.00000	0.00000	2.00000
0	1	1	1	0.43750	0.62500	0.00000	1.00000	0.00000	3.00000
1	0	0	0	0.50000	0.50000	0.00000	-3.00000	0.00000	0.00000
1	0	0	1	0.56250	0.62500	0.00000	1.00000	0.00000	1.00000
1	0	1	0	0.62500	0.75000	0.00000	1.00000	0.00000	2.00000
1	0	1	1	0.68750	0.87500	0.00000	1.00000	0.00000	3.00000
1	1	0	0	0.75000	0.75000	0.00000	-3.00000	0.00000	0.00000
1	1	0	1	0.81250	0.87500	0.00000	1.00000	0.00000	1.00000
1	1	1	0	0.87500	1.00000	0.00000	1.00000	0.00000	2.00000
1	1	1	1	0.93750	1.12500	0.00000	1.00000	0.00000	3.00000

$\therefore$ $INL = +3LSB$ and $0\ LSB$. $DNL = +1LSB$ and $-3LSB$. Nonmontonic because $DNL < 1LSB$.

$k = 6$:

$$\frac{v_{OUT}}{V_{REF}} = \frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{12} + \frac{b_3}{24}$$

The result is on the next page:

Problem 10.3-01 – Continued

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.04167	0.00000	-0.33333	0.00000	-0.33333
0	0	1	0	0.12500	0.08333	0.00000	-0.33333	0.00000	-0.66667
0	0	1	1	0.18750	0.12500	0.00000	-0.33333	0.00000	-1.00000
0	1	0	0	0.25000	0.25000	0.00000	1.00000	0.00000	0.00000
0	1	0	1	0.31250	0.29167	0.00000	-0.33333	0.00000	-0.33333
0	1	1	0	0.37500	0.33333	0.00000	-0.33333	0.00000	-0.66667
0	1	1	1	0.43750	0.37500	0.00000	-0.33333	0.00000	-1.00000
1	0	0	0	0.50000	0.50000	0.00000	1.00000	0.00000	0.00000
1	0	0	1	0.56250	0.54167	0.00000	-0.33333	0.00000	-0.33333
1	0	1	0	0.62500	0.58333	0.00000	-0.33333	0.00000	-0.66667
1	0	1	1	0.68750	0.62500	0.00000	-0.33333	0.00000	-1.00000
1	1	0	0	0.75000	0.75000	0.00000	1.00000	0.00000	0.00000
1	1	0	1	0.81250	0.79167	0.00000	-0.33333	0.00000	-0.33333
1	1	1	0	0.87500	0.83333	0.00000	-0.33333	0.00000	-0.66667
1	1	1	1	0.93750	0.87500	0.00000	-0.33333	0.00000	-1.00000

$\therefore$ $INL = +0LSB$ and $-1\ LSB$. $DNL = +1LSB$ and $-0.333LSB$. Montonic because $DNL > -0.333LSB$.

Problem 10.3-02

Repeat Problem 10.3-1 if the divisor is 3 and 5.

Solution

k=3: $v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF} + \left(\frac{b_2}{2} + \frac{b_3}{4}\right)\frac{V_{REF}}{3} = \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{6} + \frac{b_3}{12}\right]V_{REF}$

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.08333	0.00000	0.33333	0.00000	0.33333
0	0	1	0	0.12500	0.16667	0.00000	0.33333	0.00000	0.66667
0	0	1	1	0.18750	0.25000	0.00000	0.33333	0.00000	1.00000
0	1	0	0	0.25000	0.25000	0.00000	-1.00000	0.00000	0.00000
0	1	0	1	0.31250	0.33333	0.00000	0.33333	0.00000	0.33333
0	1	1	0	0.37500	0.41667	0.00000	0.33333	0.00000	0.66667
0	1	1	1	0.43750	0.50000	0.00000	0.33333	0.00000	1.00000
1	0	0	0	0.50000	0.50000	0.00000	-1.00000	0.00000	0.00000
1	0	0	1	0.56250	0.58333	0.00000	0.33333	0.00000	0.33333
1	0	1	0	0.62500	0.66667	0.00000	0.33333	0.00000	0.66667
1	0	1	1	0.68750	0.75000	0.00000	0.33333	0.00000	1.00000
1	1	0	0	0.75000	0.75000	0.00000	-1.00000	0.00000	0.00000
1	1	0	1	0.81250	0.83333	0.00000	0.33333	0.00000	0.33333
1	1	1	0	0.87500	0.91667	0.00000	0.33333	0.00000	0.66667
1	1	1	1	0.93750	1.00000	0.00000	0.33333	0.00000	1.00000

From the above table, INL = +1LSB and –0LSB, DNL = +0.33LSB and –1LSB. The DAC is on the threshold of nonmonotonicity.

k=5: $v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF} + \left(\frac{b_2}{2} + \frac{b_3}{4}\right)\frac{V_{REF}}{5} = \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{10} + \frac{b_3}{20}\right]V_{REF}$

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.05000	0.00000	-0.20000	0.00000	-0.20000
0	0	1	0	0.12500	0.10000	0.00000	-0.20000	0.00000	-0.40000
0	0	1	1	0.18750	0.15000	0.00000	-0.20000	0.00000	-0.60000
0	1	0	0	0.25000	0.25000	0.00000	0.60000	0.00000	0.00000
0	1	0	1	0.31250	0.30000	0.00000	-0.20000	0.00000	-0.20000
0	1	1	0	0.37500	0.35000	0.00000	-0.20000	0.00000	-0.40000
0	1	1	1	0.43750	0.40000	0.00000	-0.20000	0.00000	-0.60000
1	0	0	0	0.50000	0.50000	0.00000	0.60000	0.00000	0.00000
1	0	0	1	0.56250	0.55000	0.00000	-0.20000	0.00000	-0.20000
1	0	1	0	0.62500	0.60000	0.00000	-0.20000	0.00000	-0.40000
1	0	1	1	0.68750	0.65000	0.00000	-0.20000	0.00000	-0.60000
1	1	0	0	0.75000	0.75000	0.00000	0.60000	0.00000	0.00000
1	1	0	1	0.81250	0.80000	0.00000	-0.20000	0.00000	-0.20000
1	1	1	0	0.87500	0.85000	0.00000	-0.20000	0.00000	-0.40000
1	1	1	1	0.93750	0.90000	0.00000	-0.20000	0.00000	-0.60000

From the above table, INL = +0LSB and –0.6LSB, DNL = +0.6LSB and –0.2LSB. The DAC is monotonic.

Problem 10.3-03

Repeat Problem 1 if the divisor is correct (4) and the V_{REF} for the *MSB* subDAC is $0.75V_{REF}$ and the V_{REF} for the *LSB* subDAC is $1.25V_{REF}$.)

Soluiton

The analog output can be written as,

$$v_{OUT} = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)\frac{3V_{REF}}{4} + \left(\frac{b_2}{2} + \frac{b_3}{4}\right)\frac{5V_{REF}}{4} = \left[\frac{3b_0}{8} + \frac{3b_1}{16} + \frac{5b_2}{32} + \frac{5b_3}{64}\right]V_{REF}$$

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.07813	0.00000	0.25000	0.00000	0.25000
0	0	1	0	0.12500	0.15625	0.00000	0.25000	0.00000	0.50000
0	0	1	1	0.18750	0.23438	0.00000	0.25000	0.00000	0.75000
0	1	0	0	0.25000	0.18750	0.00000	-1.75000	0.00000	-1.00000
0	1	0	1	0.31250	0.26563	0.00000	0.25000	0.00000	-0.75000
0	1	1	0	0.37500	0.34375	0.00000	0.25000	0.00000	-0.50000
0	1	1	1	0.43750	0.42188	0.00000	0.25000	0.00000	-0.25000
1	0	0	0	0.50000	0.37500	0.00000	-1.75000	0.00000	-2.00000
1	0	0	1	0.56250	0.45313	0.00000	0.25000	0.00000	-1.75000
1	0	1	0	0.62500	0.53125	0.00000	0.25000	0.00000	-1.50000
1	0	1	1	0.68750	0.60938	0.00000	0.25000	0.00000	-1.25000
1	1	0	0	0.75000	0.56250	0.00000	-1.75000	0.00000	-3.00000
1	1	0	1	0.81250	0.64063	0.00000	0.25000	0.00000	-2.75000
1	1	1	0	0.87500	0.71875	0.00000	0.25000	0.00000	-2.50000
1	1	1	1	0.93750	0.79688	0.00000	0.25000	0.00000	-2.25000

From the above table, INL = +0.75LSB and –3LSB, DNL = +0.25LSB and –1.75LSB. The DAC is not monotonicity.

Problem 10.3-04

Find the worst case tolerance of x ($\Delta x/x$) in % that will not cause a conversion error for the DAC shown. Assume that all aspects of the DAC are ideal except for x. (Note: that the divisor is $1/x$ so that x is less than 1.)

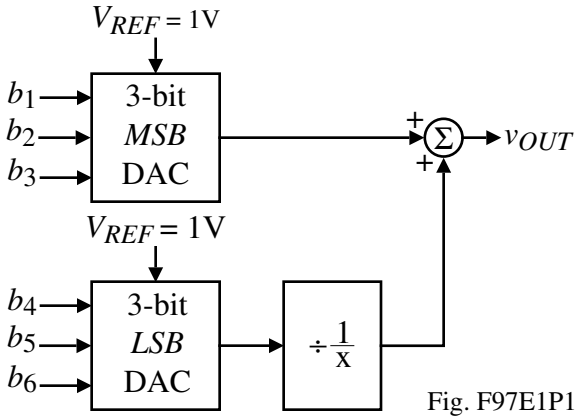


Fig. F97E1P1

Solution

The tolerance is only influenced by the bits of the *LSB* DAC. The ideal and actual outputs are given as,

$$v_{out}(\text{ideal}) = x\left[\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8}\right]$$

$$v_{out}(\text{actual}) = (x \pm \Delta x)\left[\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8}\right]$$

$$\therefore \text{ Worst case error} = |v_{out}(\text{actual}) - v_{out}(\text{ideal})| \le 1/2^7 \Rightarrow \Delta x\left[\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8}\right] \le \frac{1}{2^7} = \frac{1}{128}$$

The tolerance is decreased if all *LSB* bits are 1. Therefore,

$$\Delta x\left(\frac{7}{8}\right) \le \frac{1}{128} \Rightarrow \qquad \Delta x \le \frac{8}{7}\frac{1}{128} = \frac{1}{112}$$

Therefore, the factor x can be expressed as,

$$x \pm \Delta x = \frac{1}{8} \pm \frac{1}{112} = \frac{14}{112} \pm \frac{1}{112}$$

The tolerance of x is expressed as

$$\boxed{\text{Tolerance of } x = \frac{\pm \Delta x}{x} = \frac{\pm 1}{14} = \pm 7.143\%}$$

Problem 10.3-05

The DAC of Fig. 10.3-2 has $m = 3$ and $k = 3$. Find (a.) the ideal value of the divisor of V_{REF} designated as x. (b.) Find the largest value of x that causes a 1*LSB DNL*. (c.) Find the smallest value of x that causes a 2*LSB DNL*.

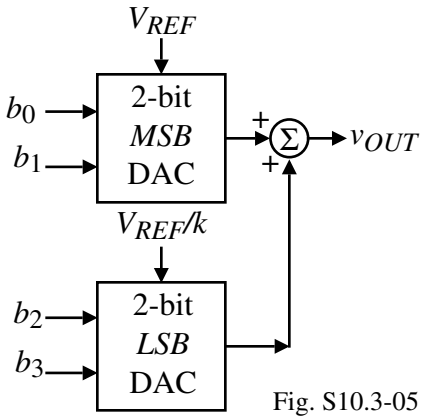


Fig. S10.3-05

Solution

a.) $v_{OUT} = V_{REF}\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{2k} + \frac{b_3}{4k}\right]$

$\underline{\underline{k = 4}}$ for ideal behavior.

b.) Let $v_{OUT}' = v_{OUT}$ when $k \neq 4$. Also note that ±1LSB = 1/16 when v_{OUT} is normalized to V_{REF}.

$$\therefore \quad \frac{v_{OUT}' - v_{OUT}}{V_{REF}} = \pm\frac{1}{16}$$

$$\left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{1}{k}\left(\frac{b_2}{2} + \frac{b_3}{4}\right)\right] - \left[\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right] = \left(\frac{1}{k} - \frac{1}{4}\right)\left(+\frac{b_2}{2} + \frac{b_3}{4}\right) = \pm\frac{1}{16}$$

$$\left(\frac{4}{k} - 1\right)(2b_2 + b_3) = \pm 1 \rightarrow \quad \frac{4}{k} = 1 \pm \left(\frac{1}{2b_2 + b_3}\right) = \frac{2b_2 + b_3 \pm 1}{2b_2 + b_3}$$

$$\therefore \quad k = \frac{4(2b_2 + b_3)}{2b_2 + b_3 \pm 1}$$

Try various combinations of b_2 and b_3:

$b_2 = 0$ and $b_3 = 1$ $\rightarrow$ $k = \frac{4}{1\pm1} = 2, \infty$

$b_2 = 1$ and $b_3 = 0$ $\rightarrow$ $k = \frac{8}{2\pm1} = \frac{8}{3}, 8$

$b_2 = 1$ and $b_3 = 1$ $\rightarrow$ $k = \frac{12}{3\pm1} = 4, 6$

The smallest, largest value of k that maintains ±1LSB is 6. $\therefore$ $\underline{\underline{k = 6}}$
(k is ideally 4 and the smallest of the maximum values is 6)

c.) For DNL, the worst case occurs from X011 to X100.

$$\therefore \quad \frac{v_{OUT}(\text{X100}) - v_{OUT}(\text{X011})}{V_{REF}/16} - 1 = \pm 2$$

$$\frac{1}{4} - \left(\frac{1}{2k} + \frac{1}{4k}\right) = \frac{1}{16} \pm \frac{2}{16} \quad \rightarrow \quad 4 - \frac{12}{k} = 1 \pm 2 \quad \rightarrow \quad \frac{12}{k} = 3 - (\pm 2)$$

$$k = \frac{12}{3-(\pm 2)} = 12 \text{ or } 2.4 \qquad \therefore \ \underline{\underline{k = 2.4}}$$

Problem 10.3-06

Show for the results of Ex. 10.3-2 that the resulting *INL* and *DNL* will be equal to –0.5*LSB* or less.

Solution

Consider only the *LSBs* because the error in the division factor only affects the *LSB* subDAC.

INL:

The worst case *INL* occurs when both b_3 and b_4 are on. Therefore,

$$\left(\frac{1}{2}+\frac{1}{4}\right)\left(\frac{6\pm1}{24}\right)=\left(\frac{3}{4}\right)\left(\frac{6\pm1}{24}\right)=\frac{6\pm1}{32}=\frac{5}{32},\frac{7}{32}$$

$$INL^{+}(\max)=V_o(\text{actual})-V_o(\text{ideal})=\frac{7}{32}-\frac{6}{32}=\frac{1}{32}=+0.5LSB$$

$$INL^{-}(\max)=V_o(\text{actual})-V_o(\text{ideal})=\frac{5}{32}-\frac{6}{32}=\frac{-1}{32}=-0.5LSB$$

Therefore, the worst case *INL* is equal to or less than ±0.5*LSB*.

DNL:

The worst case *DNL* occurs when both bits of the *LSB* subDAC change from 1 to 0. This corresponds to a change from 0011 to 0100. If the scaling factor is 7/24 corresponding to the +1/24 tolerance, then

$$\Delta V_o=V_o(0011)-V_o(0100)=\frac{5}{32}-\frac{1}{4}=\frac{5}{32}-\frac{8}{32}=\frac{3}{32}$$

$$DNL^{+}=\Delta V_o-\frac{2}{32}=\frac{3}{32}-\frac{2}{32}=\frac{1}{32}=+0.5LSB$$

If the scaling factor is 5/24 corresponding to the -1/24 tolerance, then

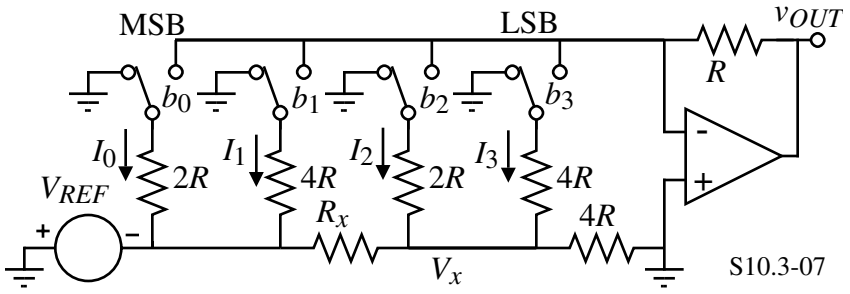
$$\Delta V_o=V_o(0011)-V_o(0100)=\frac{7}{32}-\frac{1}{4}=\frac{7}{32}-\frac{8}{32}=\frac{1}{32}$$

$$DNL^{-}=\Delta V_o-\frac{2}{32}=\frac{1}{32}-\frac{2}{32}=\frac{-1}{32}=-0.5LSB$$

Therefore, the worst case *DNL* is equal to or less than ±0.5*LSB*.

Problem 10.3-07

A 4-bit, digital-analog converter is shown in Fig. P10.3-7. When a bit is 1, the switch pertaining to that bit is connected to the op amp negative input terminal, otherwise it is connected to ground. Identify the switches by the notation b_1, b_2, b_3, or b_4 where b_i corresponds to the ith bit and b_1 is the *MSB* and b_4 is the *LSB*. Solve for the value of R_x which will give proper digital-analog converter performance.



Solution

For this circuit to operate properly, $I_0 = \frac{V_{REF}}{2R}$, $I_1 = \frac{I_0}{2}$, $I_2 = \frac{I_0}{4}$, and $I_3 = \frac{I_0}{8}$.

To achieve this result, $V_x = -\frac{V_{REF}}{4}$. The equivalent resistance seen to ground from the right of R_x can be expressed as,

$$R_{EQ} = 2R||(4R||4R) = 2R||2R = R$$

$$\therefore \quad V_x = \frac{R}{R+R_x}(-V_{REF}) = -\frac{V_{REF}}{4}$$

$$\therefore \quad \boxed{R_x = 3R}$$

Problem 10.3-08

Assume $R_1=R_5=2R$, $R_2=R_6=4R$, $R_3=R_7=8R$, $R_4=R_8=16R$ and that the op amp is ideal. (a.) Find the value of R_9 and R_{10} in terms of R which gives an ideal 8-bit digital-to-analog converter. (b.) Find the range of values of R_9 in terms of R which keeps the $INL \le \pm 0.5LSB$. Assume that R_{10} has its ideal value. Clearly state any assumption you make in working this problem. (c.) Find the range of R_{10} in terms of R which keeps the converter monotonic. Assume that R_9 has its ideal value. Clearly state any assumptions you make in working this problem.

Solution

(a.) $\boxed{R_8 = 16R \text{ and } R_9 = R}$

(b.) $$v_{OUT} = V_{REF}\left(\frac{b_0}{2} + \frac{b_1}{4} + \frac{b_2}{8} + \frac{b_3}{16}\right) + \frac{R}{R_8}V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)$$

The worst case INL occurs when the bits in the MSB subDAC are zero and the bits in the LSB subDAC are one.

$$\therefore \quad v_{OUT} = \frac{R}{R_8}V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)$$

$$v_{OUT}(\text{ideal}) = \frac{1}{16}V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)$$

$$\therefore \quad \text{INL} = v_{OUT} - v_{OUT}(\text{ideal}) = V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)\left(\frac{R}{R_8} - \frac{1}{16}\right) = +\frac{1}{2}\frac{V_{REF}}{256}$$

$$512(0.9375)\left(\frac{R}{R_8} - \frac{1}{16}\right) = 1 \quad \rightarrow \quad \frac{R}{R_8} = 0.064583 \quad \rightarrow \quad R_8 = 15.4838R$$

Also, $$\text{INL} = v_{OUT} - v_{OUT}(\text{ideal}) = V_{REF}\left(\frac{b_4}{2} + \frac{b_5}{4} + \frac{b_6}{8} + \frac{b_7}{16}\right)\left(\frac{R}{R_8} - \frac{1}{16}\right) = -\frac{1}{2}\frac{V_{REF}}{256}$$

$$512(0.9375)\left(\frac{R}{R_8} - \frac{1}{16}\right) = -1 \quad \rightarrow \quad \frac{R}{R_8} = 0.060417 \rightarrow \quad R_8 = 16.5517R$$

$$\therefore \quad \boxed{15.4838R \le R_8 \le 16.5517R}$$

(c.) Worst case monotonicity occurs when the bits of the LSB subDAC go from 1 to 0.

$$v_{OUT}(\text{LSBs} = 1) = \frac{V_{REF}}{16}\left(\frac{1}{2} + \frac{1}{4} + \frac{1}{8} + \frac{1}{16}\right) = \frac{V_{REF}}{16}\left(\frac{15}{16}\right)$$

$$v_{OUT}(b_3 = 1, \text{ all others } 0) = V_{REF}\frac{R}{R_9}\left(\frac{1}{16}\right)$$

Nonmonotonicity $\Rightarrow$ $$V_{REF}\frac{R}{R_9}\left(\frac{1}{16}\right) > \frac{V_{REF}}{16}\left(\frac{15}{16}\right) \quad \rightarrow \quad \boxed{R_9 < \frac{15}{16}R}$$

Problem 10.3-09

Design a ten-bit, two-stage charge-scaling D/A converter similar to Fig. 10.3-4 using two five-bit sections with a capacitive attenuator between the stages. Give all capacitances in terms of *C*, which is the smallest capacitor of the design.

Solution

The result is shown below.

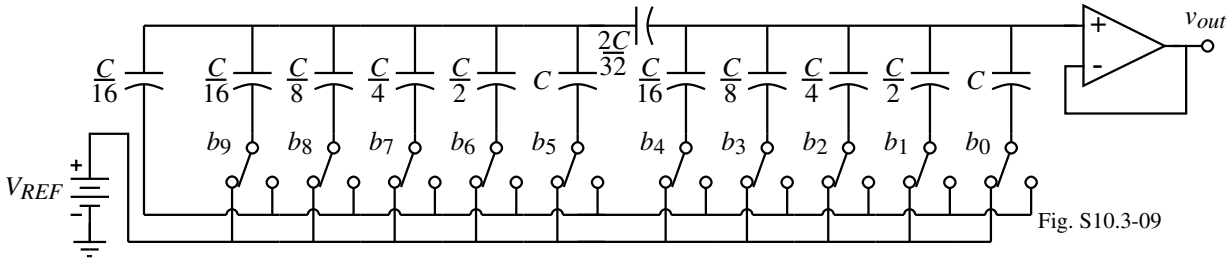


Fig. S10.3-09

The design of the connecting capacitor, C_s, is done as follows,

$$\frac{C}{16} = \frac{1}{\frac{1}{C_s} + \frac{1}{2C}} \rightarrow \quad \frac{1}{C_s} + \frac{1}{2C} = \frac{16}{C} \quad \rightarrow \quad \frac{1}{C_s} = \frac{32}{2C} - \frac{1}{2C} = \frac{31}{2C}$$

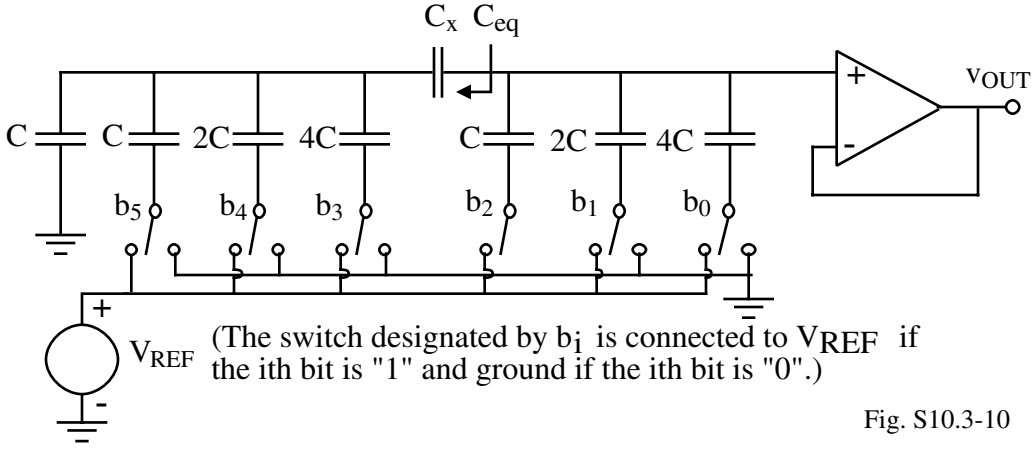
$$\therefore \quad C_s = \frac{2C}{31}$$

Problem 10.3-10

A two-stage, charge-scaling D/A converter is shown in Fig. P10.3-10. (a.) Design C_x in terms of C, the unit capacitor, to achieve a 6-bit, two-stage, charge-scaling DAC. (b.) If C_x is in error by ΔC_x, find an expression for v_{OUT} in terms of C_x, ΔC_x, b_i and V_{REF}. (c.) If the expression for v_{OUT} in part (b.) is given as

$$v_{OUT} = \frac{V_{REF}}{8}\left(1 - \frac{17\Delta C_x}{100C_x}\right)\left[\sum_{i=1}^{3} b_i 2^{3-i} + \left(1 + \frac{8\Delta C_x}{10C_x}\right)\sum_{i=4}^{6}\frac{b_i 2^{6-i}}{8}\right]$$

what is the accuracy of C_x necessary to avoid an error using worst case considerations.



(The switch designated by b_i is connected to V_{REF} if the ith bit is "1" and ground if the ith bit is "0".)

Fig. S10.3-10

Solution

(a.) The value of C_{eq}. must be C. Therefore,

$$\frac{1}{C} = \frac{1}{C_x} + \frac{1}{8C} \quad \rightarrow \quad \frac{1}{C_x} = \frac{7}{8C} \quad \rightarrow \quad \boxed{C_x = \frac{8C}{7}}$$

(b.) The model for the analysis is found by using Thevenin's equivalent circuits and is ,

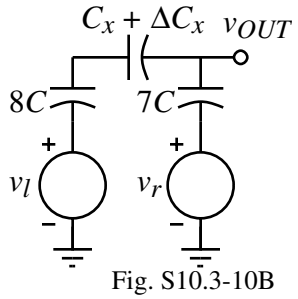


Fig. S10.3-10B

$$v_r = \sum_{i=0}^{2}\frac{b_i 2^{2-i}}{7}V_{REF}$$

$$v_l = \sum_{i=3}^{5}\frac{b_i 2^{5-i}}{8}V_{REF}$$

$$v_{OUT} = \left(\frac{\frac{1}{8C} + \frac{1}{C_x+\Delta C_x}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x+\Delta C_x}}\right)v_r + \left(\frac{\frac{1}{7C}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x+\Delta C_x}}\right)v_l$$

Problem 10.3-10 – Continued

$$v_{OUT} = \left(\frac{\frac{1}{8C} + \frac{1}{C_x(1+\Delta C_x/C_x)}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x(1+\Delta C_x/C_x)}} \right) v_r + \left(\frac{\frac{1}{7C}}{\frac{1}{8C} + \frac{1}{7C} + \frac{1}{C_x(1+\Delta C_x/C_x)}} \right) v_l$$

Let $C_x = \frac{8C}{7}$ and $\frac{\Delta C_x}{C_x} = \varepsilon$

$$\therefore \quad v_{OUT} = \left(\frac{\frac{1}{8C} + \frac{7}{8C}\left(\frac{1}{1+\varepsilon}\right)}{\frac{1}{8C} + \frac{1}{7C} + \frac{7}{8C}\left(\frac{1}{1+\varepsilon}\right)} \right) v_r + \left(\frac{\frac{1}{7C}}{\frac{1}{8C} + \frac{1}{7C} + \frac{7}{8C}\left(\frac{1}{1+\varepsilon}\right)} \right) v_l$$

Assume that $\frac{1}{1+\varepsilon} \approx 1-\varepsilon$ to get,

$$v_{OUT} \approx \left(\frac{\frac{1}{8} + \frac{7}{8} - \frac{7\varepsilon}{8}}{\frac{1}{8} + \frac{1}{7} + \frac{7}{8} - \frac{7\varepsilon}{8}} \right) v_r + \left(\frac{\frac{1}{7}}{\frac{1}{8} + \frac{1}{7} + \frac{7}{8} - \frac{7\varepsilon}{8}} \right) v_l = \left(\frac{1 - \frac{7\varepsilon}{8}}{1 + \frac{1}{7} - \frac{7\varepsilon}{8}} \right) v_r + \left(\frac{\frac{1}{7}}{1 + \frac{1}{7} - \frac{7\varepsilon}{8}} \right) v_l$$

$$v_{OUT} = \left(\frac{7 - \frac{49\varepsilon}{8}}{8 - \frac{49\varepsilon}{8}} \right) v_r + \left(\frac{1}{8 - \frac{49\varepsilon}{8}} \right) v_l = \frac{7}{8}\left(\frac{1 - \frac{49\varepsilon}{56}}{1 - \frac{49\varepsilon}{64}} \right) v_r + \frac{1}{8\left(1 - \frac{49\varepsilon}{64}\right)} v_l$$

$$v_{OUT} = \frac{7}{8}\left(\frac{1 - \frac{49\varepsilon}{56}}{1 - \frac{49\varepsilon}{64}} \right)\left(v_r + \frac{v_l}{7\left(1 - \frac{49\varepsilon}{56}\right)} \right) \approx \frac{7}{8}\left[1 + \left(\frac{49}{64} - \frac{49}{56}\right)\varepsilon \right]\left(v_r + \frac{1}{7}\left(1 + \frac{49\varepsilon}{56}\right) v_l \right)$$

$$v_{OUT} = \frac{7}{8}\left(1 - \frac{7\varepsilon}{64}\right)\left[\sum_{i=0}^{2} \frac{b_i 2^{2-i}}{7} V_{REF} + \frac{1}{7}\left(1 + \frac{49\varepsilon}{56}\right) \sum_{i=3}^{5} \frac{b_i 2^{5-i}}{8} V_{REF} \right]$$

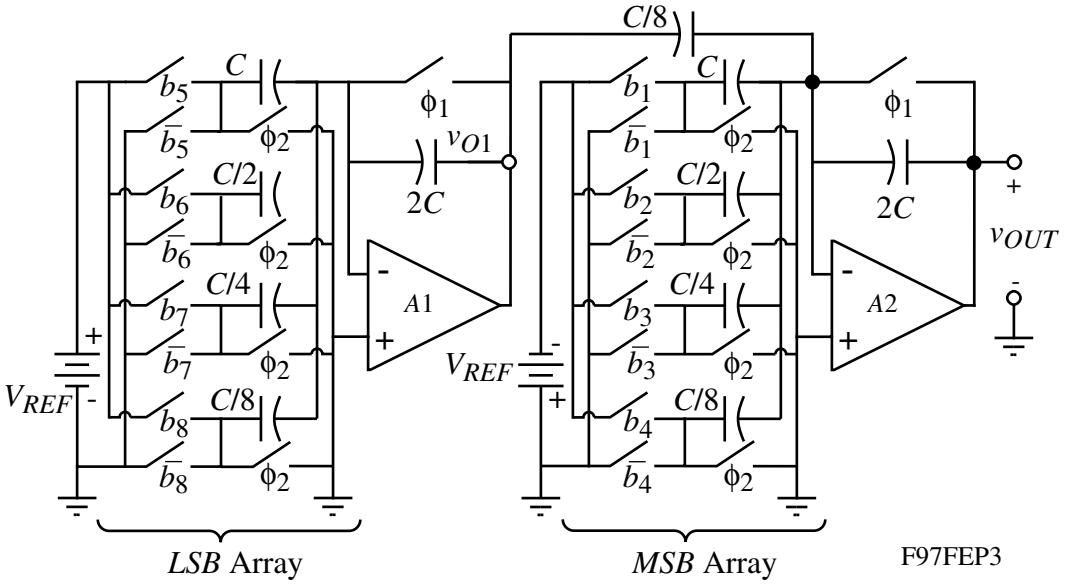
$$\therefore \quad \boxed{ v_{OUT} = \frac{V_{REF}}{8}\left(1 - \frac{7\varepsilon}{64}\right)\left[\sum_{i=0}^{2} b_i 2^{2-i} + \left(1 + \frac{7\varepsilon}{8}\right) \sum_{i=3}^{5} \frac{b_i 2^{5-i}}{8} \right] }$$

(c.) The error due to ΔC_x should be less than $\pm 0.5LSB$. Worst case is for all bits 1.

$$\therefore \quad \left(-\frac{17\Delta C_x}{100C_x} + \frac{8\Delta C_x}{10C_x} \right)\frac{7V_{REF}}{8} \le \frac{V_{REF}}{2^{N+1}} = \frac{V_{REF}}{128} \quad \rightarrow \quad \boxed{ \frac{\Delta C_x}{C_x} \le 1.685\% }$$

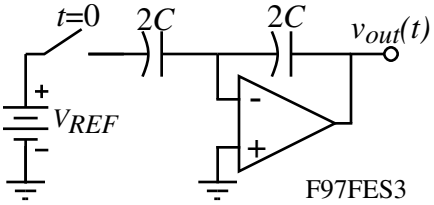
Problem 10.3-11

If the op amps in the circuit below have a dc gain of 10^4 and a dominant pole at 100Hz, at what clock frequency will the *effective number of bits (ENOB)* = 7bits assuming that the capacitors and switches are ideal? Use a worst case approach to this problem and assume that time responses of the *LSB* and *MSB* stages add to give the overall conversion time.



Solution

The worst case approach assumes that all capacitors are switched into the op amp input and that both stages can be modelled approximately as shown.



With a single pole model for the op amp, it can be shown that the -3dB frequency is given as follows where $C_1 = C_2$ gives the lowest -3dB frequency.

$$\omega_H = \frac{GB \cdot C_2}{C_1 + C_2} = \frac{GB}{2} = \pi \text{x} 10^6 \text{ radians/sec}$$

$\therefore\ v_{out}(t) = (C_1/C_2)[1 - e^{-\omega_H t}]V_{REF}$

ENOB of 7 bits $\Rightarrow$ $\pm\frac{1}{2}\frac{V_{REF}}{2^7} = \pm\frac{V_{REF}}{2^8}$ $v_{out}(T) = V_{REF} - \frac{V_{REF}}{2^8}$

$$\therefore\ 1 - \frac{1}{2^8} = 1 - e^{-\omega_H T} \Rightarrow e^{\omega_H T} = 2^8 \Rightarrow T = \frac{8}{\omega_H} ln(2) = \frac{8}{\pi \text{x} 10^6} 0.693 = 1.765\mu\text{s}$$

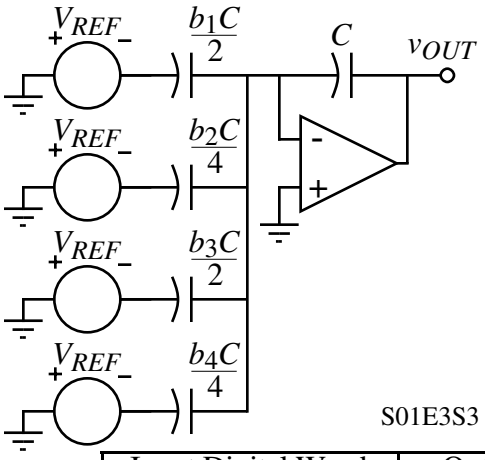
Double this time for 2 stages to $T_{clock} = 3.53\mu\text{s}$ $\Rightarrow$ $\boxed{f_{clock} = \frac{1}{T_{clock}} = 283\text{kHz}}$

Problem 10.3-12

The DAC shown uses two identical, 2-bit DACs to achieve a 4-bit D/A converter. Give an expression for v_{OUT} as a function of V_{REF} and the bits, b_1, b_2, b_3, and b_4 during the ϕ_2 phase period. The switches controlled by the bits are closed if the bit is high and open if the bit is low during the ϕ_2 phase period. If k = 2, express the INL (in terms of a ±LSB value) and DNL (in terms of a ±LSB value) and determine whether the converter is monotonic or not. (You may use the output-input plot on the next page if you wish.)

Solution

During the ϕ_2 phase the DAC can be modeled as:



S01E3S3

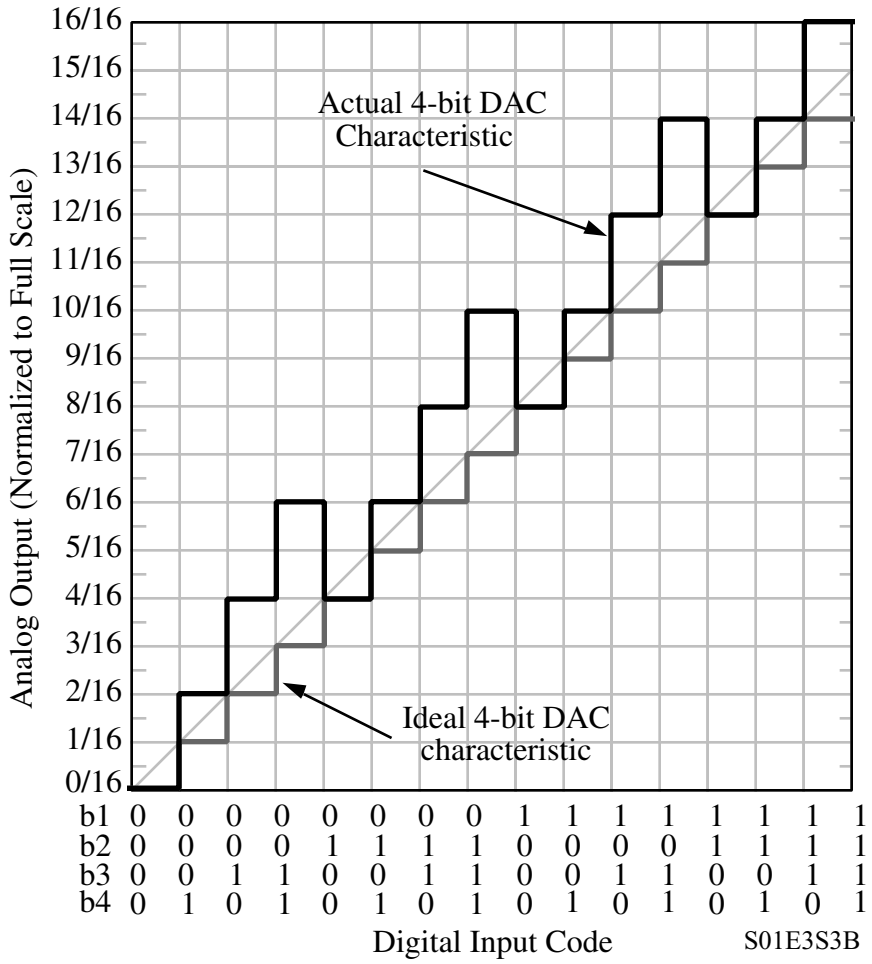
$$v_{OUT}(\phi_2) = \left[\left(\frac{b_1}{2} + \frac{b_2}{4}\right) + \frac{1}{k}\left(\frac{b_2}{2} + \frac{b_4}{4}\right)\right] V_{REF}$$

If $k = 2$, then

$$\frac{v_{OUT}(\phi_2)}{V_{REF}} = \frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{4} + \frac{b_4}{8}$$

Input Digital Word	Output for $k = 4$	Output for $k = 2$
0000	0	0
0001	1/16	2/16
0010	2/16	4/16
0011	3/16	6/16
0100	4/16	4/16
0101	5/16	6/16
0110	6/16	8/16
0111	7/16	10/16
1000	8/16	8/16
1001	9/16	10/16
1010	10/16	12/16
1011	11/16	14/16
1100	12/16	12/16
1101	13/16	14/16
1110	14/16	16/16
1111	15/16	18/16

Problem 10.3-12 – Continued



The INL is +3LSB and –0LSB.

The DNL is +1LSB and –3LSB.

Converter is definitely not monotonic.

Problem 10.3-13

An *N*-bit DAC consists of a voltage scaling DAC of *M*-bits and a charge scaling DAC of *K*-bits (*N*=*M*+*K*). The accuracy of the resistors in the *M*-bit voltage scaling DAC is $-\Delta R/R$. The accuracy of the binary-weighted capacitors in the charge scaling DAC is $-\Delta C/C$. Assume for this problem that *INL* and *DNL* can be expressed generally as,

INL = Accuracy of component x Maximum weighting factor

DNL = Accuracy of the largest component x Corresponding weighting factor

where the weighting factor for the *i-th* bit is 2^{N-i+1}.

(a.) If the *MSB* bits use the *M*-bit voltage scaling DAC and the *LSB* bits use the *K*-bit charge scaling DAC, express the *INL* and *DNL* of the N-bit DAC in terms of *M*, *K*, *N*, $\Delta R/R$, and $\Delta C/C$. (b.) If the *MSB* bits use the *K*-bit charge scaling DAC and the *LSB* bits use the *M*-bit voltage scaling DAC, express the *INL* and *DNL* of the N-bit DAC in terms of *M*, *K*, *N*, $\Delta R/R$, and $\Delta C/C$.

Solution

(a.) In a *M*-bit voltage scaling DAC, there are 2^M resistors between V_{REF} and ground. The voltage at the bottom of the *i*-th resistor from the top is $v_i = \dfrac{(2^M\text{-}i)R}{(2^M\text{-}i)R + iR} V_{REF}$ where the iR resistors are above v_i and the $2^M\text{-}i$ resistors are below v_i. The worst case $INL(R)$ for the voltage scaling DAC is found at the midpoint where $i = 2^{M-1}$ and the resistors below are all maximum positive and the resistors above are all maximum negative. Thus,

$$INL(R) = v_{2^{M-1}}(\text{actual}) - v_{2^{M-1}}(\text{ideal}) = \frac{2^{M-1}(R+\Delta R)V_{REF}}{2^{M-1}(R+\Delta R) + 2^{M-1}(R-\Delta R)} - \frac{V_{REF}}{2} = \frac{\Delta R}{2R}$$

or

$$\boxed{INL(R) = \frac{2^M}{2^M}\left(\frac{\Delta R}{2R}\right) = 2^{M-1}\frac{\Delta R}{R}\ \text{LSBs}}$$

The worst case $DNL(R)$ for the voltage scaling DAC is found as the maximum step size minus the ideal step size. Thus,

$$DNL(R) = v_{step}(\text{actual}) - v_{step}(\text{ideal}) = \frac{(R\pm\Delta R)V_{REF}}{2^M R} - \frac{R}{2^M R} V_{REF} = \frac{\pm\Delta R}{2^M R} V_{REF}$$

or

$$\boxed{DNL(R) = \left(\frac{\pm\Delta R\ V_{REF}}{2^M R}\right)\frac{2^N}{2^N} = \frac{\pm 2^N}{2^M}\frac{\Delta R}{R} = \pm 2^K \frac{\Delta R}{R}\ \text{LSBs}}$$

Let us now examine the $INL(C)$ and the $DNL(C)$ of a *K*-bit binary-weighted capacitor array. The ideal output for the *i*-th capacitor is given as

$$v_{OUT}(\text{ideal}) = \frac{C/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i}\left(\frac{2^K}{2^K}\right) = \frac{2^K}{2^i}\ LSBs$$

The actual wors-case output for the *i*-th capacitor is given as

$$v_{OUT}(\text{actual}) = \frac{(C\pm\Delta C)/2^{i-1}}{2C} V_{REF} = \frac{V_{REF}}{2^i} \pm \frac{\Delta C \cdot V_{REF}}{2^i C} = \frac{2^K}{2^i} \pm \frac{2^K \Delta C}{2^i C}\ LSBs$$

Problem 10.3-13 — Continued

Therefore, the *INL* due to the binary-weighted capacitor array is

$$INL(C) = v_{OUT}(\text{actual}) - v_{OUT}(\text{ideal}) = \pm\frac{2^K\Delta C}{2^i C} = \pm\frac{2^{K-i}\Delta C}{C}\ LSBs$$

The worst case occurs for $i = 1$ which gives $\boxed{INL(C) = \pm\frac{2^{K-1}\Delta C}{C}\ LSBs}$

Finally, the worst case *DNL* due to the binary-weighted capacitor array is found as

$$DNL(C) = v_{OUT}(1000\ldots.) - v_{OUT}(0111\ldots.) = \frac{2^{K-1}\Delta C}{C} + \frac{2^{K-1}\Delta C}{C} = \frac{2^K\Delta C}{C}\ LSBs$$

The *INL* when the *MSBs* use voltage scaling and the *LSBs* use charge scaling is,

$$\boxed{INL = INL(R) + INL(C) = 2^{M-1}\frac{\Delta R}{R} + 2^{N-1}\frac{\Delta C}{C}}$$

where the *LSB* of the charge scaling DAC is now $VREF/2^N$ rather than $VREF/2^K$.

The *DNL* when the *MSBs* use voltage scaling and the *LSBs* use charge scaling is,

$$\boxed{DNL = DNL(R) + DNL(C) = 2^K\frac{\Delta R}{R} + 2^K\frac{\Delta C}{C} = 2^K\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)}$$

(b.) Fortunately we can use the above results for the case where the *MSBs* use the charge-scaling DAC and the *LSBs* use the voltage scaling DAC.

For *INL*(*R*) the *LSB* is now $V_{REF}/2^N$. Therefore,

$$\boxed{INL(R) = \frac{2^N}{2^N}\left(\frac{\Delta R}{2R}\right)V_{REF} = 2^{N-1}\frac{\Delta R}{R}\ LSBs}$$

For the *INL*(*C*), *K* is replaced with *N* to give,

$$\boxed{INL(C) = \pm\frac{2^{N-1}\Delta C}{C}\ LSBs}$$

For the *DNL*(*R*), the *LSB* is $V_{REF}/2^N$ so that the *DNL*(*R*) for part (b.) becomes

$$\boxed{DNL(R) = \frac{\pm\Delta R}{2^N R}V_{REF} = \frac{\pm\Delta R}{R}\ LSBs}\ )$$

Since the *MSB* for the chage scaling DAC is now *N*, the *DNL*(*C*) becomes

$$\boxed{DNL(C) = \frac{2^N\Delta C}{C}\ LSBs}$$

Combining the above results gives the *INL* and *DNL* for the case where the *MSBs* use the charge scaling DAC and the *LSBs* use the voltage DAC. The result is,

$$\boxed{INL = 2^{N-1}\left(\frac{\Delta R}{R} + \frac{\Delta C}{C}\right)LSBs}$$ and

$$\boxed{DNL = \left(2^{N-1}\frac{\Delta C}{C} + \frac{\Delta R}{R}\right)\ LSBs}$$

Problem 10.3-14

Below are the formulas for *INL* and *DNL* for the case where the MSB and LSB arrays of an digital-to-analog converter are either voltage or charge scaling. $n = m+k$, where m is the number of bits of the MSB array and k is the number of bits of the LSB array and n is the total number of bits. Find the values of n, m, and k and tell what type of DAC (voltage MSB and charge LSB or charge MSB and voltage LSB) if $\Delta R/R = 1\%$ and $\Delta C/C = 0.1\%$ and both the *INL* and *DNL* of the DAC combination should each be 1*LSB* or less.

DAC Combination	*INL* (LSBs)	*DNL* (LSBs)
MSB voltage (m-bits) LSB charge (k-bits)	$2^{n-1}\frac{\Delta R}{R} + 2^{k-1}\frac{\Delta C}{C}$	$2^{k}\frac{\Delta R}{R} + (2^{k}-1)\frac{\Delta C}{C}$
MSB charge (m-bits) LSB voltage (k-bits)	$2^{m-1}\frac{\Delta R}{R} + 2^{n-1}\frac{\Delta C}{C}$	$\frac{\Delta R}{R} + (2^{n}-1)\frac{\Delta C}{C}$

Solution

MSB voltage, *LSB* charge:

$$1 \geq 2^{n-1}\left(\frac{1}{100}\right) + 2^{k-1}\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 10\cdot 2^{n-1} + 2^{k-1}$$

$$1 \geq 2^{k}\left(\frac{1}{100}\right) + (2^{k}-1)\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 10\cdot 2^{k} + 2^{k}-1 \Rightarrow \frac{999}{11} = 90.8 \geq 2^{k} \Rightarrow \quad k = 6$$

Substituting this k into the first equation gives

$$\frac{1000 - 32}{10} = 96.8 \geq 2^{n-1} \quad \Rightarrow \quad n = 7 \text{ which gives } m = 1 \text{ and } k = 6.$$

MSB charge, *LSB* voltage:

$$1 \geq 2^{m-1}\left(\frac{1}{100}\right) + 2^{n-1}\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 5\cdot 2^{m} + 2^{n-1}$$

$$1 \geq \frac{1}{100} + (2^{n}-1)\left(\frac{1}{1000}\right) \quad \Rightarrow \quad 1000 \geq 10 + 2^{n}-1 \Rightarrow 991 \geq 2^{n} \Rightarrow \quad n = 9$$

Substituting this n into the first equation gives

$$\frac{1000 - 256}{5} = 148.8 \geq 2^{m} \quad \Rightarrow \quad m = 7 \text{ which gives } n = 9 \text{ and } k = 2.$$

Therefore, the DAC combination where the *MSBs* are charge scaling and the *LSBs* are voltage scaling gives the most bits when both *INL* and *DNL* are 1*LSB*. The number of bits is $n = 9$ with $m = 7$ bits of charge scaling for the *MSB* DAC and $k = 2$ bits of voltage scaling for the *LSB* DAC.

Problem 10.3-15

The circuit shown is a double-decoder D/A converter. Find an expression for v_X in terms of V_1, V_2, and V_{REF} when the ϕ_2 switches are closed. If A=1, B=0, C=1, and D=1, will the comparator output be high or low if $V_{analog} = 0.8V_{REF}$?

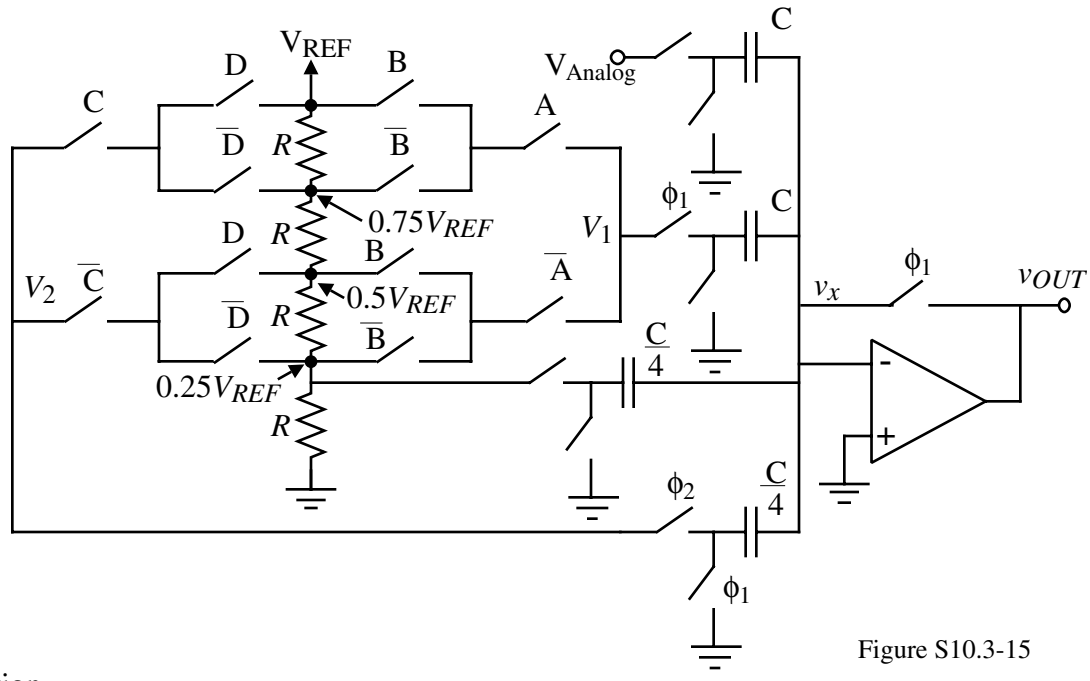


Figure S10.3-15

Solution

At ϕ_2 we have the following equivalent circuit:

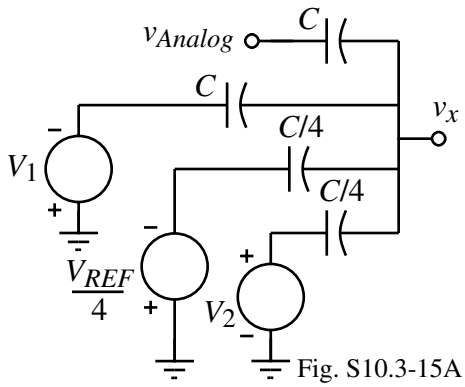


Fig. S10.3-15A

Summing the currents to zero gives,

$$sC(v_{Analog}-v_x) + sC(-V_1-v_x) + \frac{sC}{4}\left(-\frac{V_{REF}}{4} - v_x\right) + \frac{sC}{4}(V_2 - v_x) = 0$$

or

$$sCv_{Analog} - CV_1 - C\frac{V_{REF}}{16} + C\frac{V_2}{4} = v_x\left(C+C+\frac{C}{4}+\frac{C}{4}\right)$$

$$\therefore \quad \boxed{v_x = \frac{C}{C_{total}}\left(v_{Analog} - V_1 + \frac{V_2}{4} - \frac{V_{REF}}{16}\right)} = \frac{2}{5}v_{Analog} - \frac{2}{5}V_1 + \frac{V_2}{10} - \frac{V_{REF}}{16}$$

For ABCD = 1011 $\rightarrow$ $v_{Analog} - V_1 + \frac{V_2}{4} - \frac{V_{REF}}{16} = \frac{12V_{REF}}{16} - \frac{12V_{REF}}{16} + \frac{4V_{REF}}{16} - \frac{V_{REF}}{16} > 0$

Since $v_x > 0$, the comparator output will be low.

Problem 10.3-16

A 4-bit, analog-to-digital converter is shown. Clearly explain the operation of this converter for a complete conversion in a clock period-by-clock period manner, where ϕ_1 and ϕ_2 are non-overlapping clocks generated from the square ware with a period of T (i.e. ϕ_1 occurs in 0 to T/2 and ϕ_2 in T/2 to T, etc.). What will cause errors in the operation of this analog-to-digital converter?

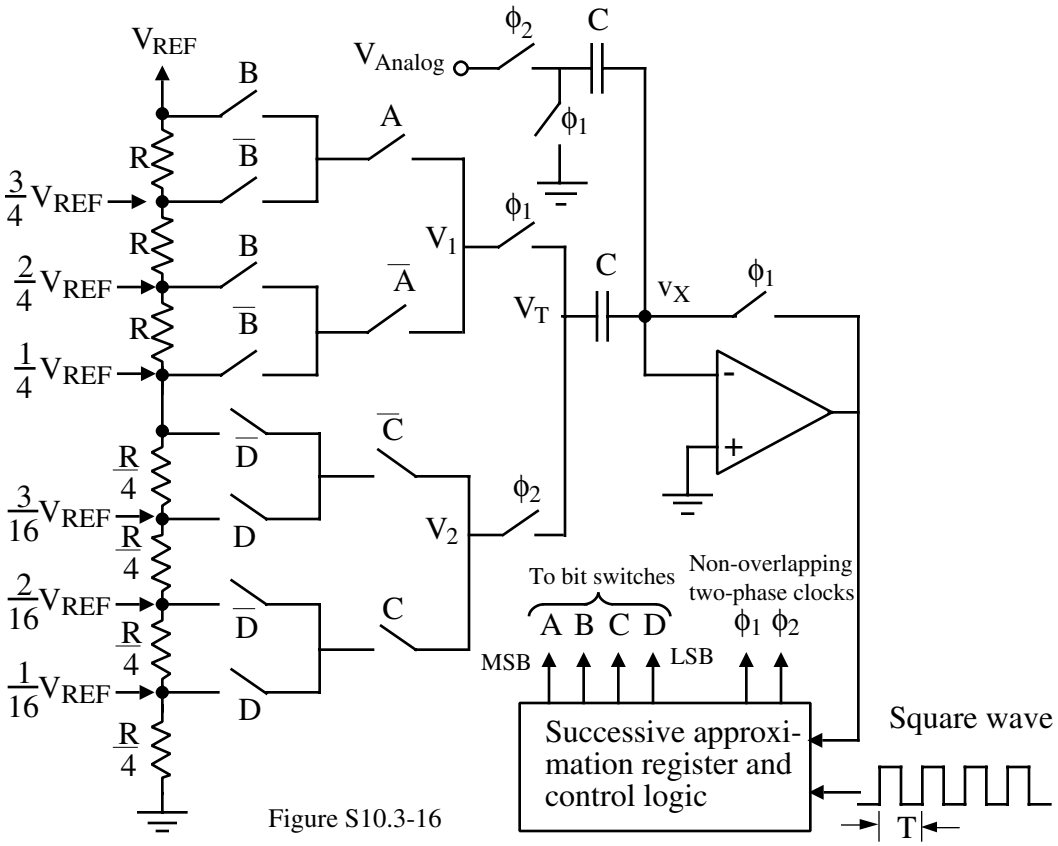


Figure S10.3-16

Solution

Consider the operation during a ϕ_1-ϕ_2 cycle. The voltage v_x can be written in general as,

$$v_x = \frac{V_{analog}}{2} - \frac{V_1}{2} + \frac{V_2}{2} = \frac{1}{2}(V_{analog} - V_1 + V_2)$$

The operation of the ADC will proceed as follows:

1.) Period 1 ($0 \le t \le T$):

SAR closes switches A, $\overline{B}$, $\overline{C}$, and $\overline{D}$ (1000) to get

$$v_x = \frac{1}{2}\left(V_{analog} - \frac{3}{8}V_{REF} + \frac{1}{8}V_{REF}\right) = \frac{1}{2}\left(V_{analog} - \frac{1}{2}V_{REF}\right)$$

If $v_x > 0$, then A = 1. Otherwise, A = 0 ($\overline{A}$ =1).

Problem 10.3-16 – Continued

2.) Period 2 ($T \le t \le 2T$):

a.) A = 1

SAR closes switches A,B , $\overline{C}$, and $\overline{D}$ (1100) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_{REF} + \frac{1}{4} V_{REF} \right) = \frac{1}{2}\left(V_{analog} - \frac{3}{4} V_{REF} \right)$$

b.) $\overline{A}$ = 1

SAR closes switches $\overline{A}$,B , $\overline{C}$, and $\overline{D}$ (0100) to get

$$v_x = \frac{1}{2}\left(V_{analog} - \frac{1}{2} V_{REF} + \frac{1}{4} V_{REF} \right) = \frac{1}{2}\left(V_{analog} - \frac{1}{4} V_{REF} \right)$$

If $v_x > 0$, the B = 1 (X100). Otherwise, B = 0 ($\overline{B}$ =1) (X000).

3.) Period 3 ($2T \le t \le 3T$):

At this point, V_1, will not change since A and B are known.

The SAR closes the appropriate A and B switches and C and $\overline{D}$ (XX10) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_1 + \frac{2}{16} V_{REF} \right) = \frac{1}{2}\left(V_{analog} - V_1 + \frac{1}{8} V_{REF} \right)$$

If $v_x > 0$, then C = 1 (XX10). Otherwise, C = 0 ($\overline{C}$ = 1) (XX00).

4.) Period 4 ($3T \le t \le 4T$):

a.) D = 1

SAR closes switches appropriate Aand B switcheds and C, and D (XX11) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_1 + \frac{1}{16} V_{REF} \right)$$

b.) $\overline{D}$ = 1

SAR closes switches appropriate Aand B switcheds and C, and $\overline{D}$ (XX10) to get

$$v_x = \frac{1}{2}\left(V_{analog} - V_1 + \frac{3}{16} V_{REF} \right)$$

If $v_x > 0$, then D = 1 (XXX1). Otherwise, D = 0 ($\overline{D}$ = 1) (XXX0).

Sources of error:

1.) Op amp/comparator – gain, GB, SR, settling time (offset not a problem).
2.) Resistor and capacitor matching.
3.) Switch resistance and feedthrough.
4.) Note parasitic capacitances.
5.) Reference accuracy and stability.

Problem 10.4-01

What is v_{C1} in Fig. 10.4-1 after the following sequence of switch closures? S_4, S_3, S_1, S_2, S_1, S_3, S_1, S_2, and S_1?

Solution

The plots for v_{C1}/V_{REF} and v_{C2}/V_{REF} are given below.

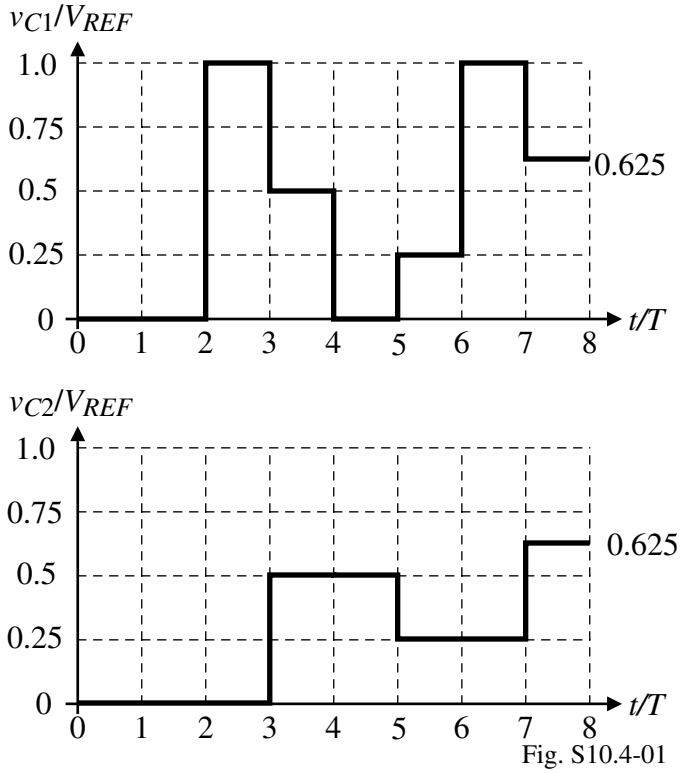


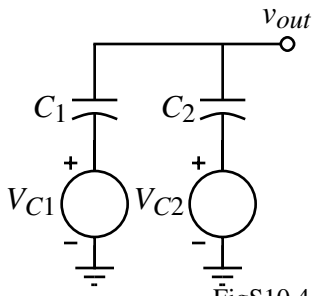
Fig. S10.4-01

Problem 10.4-02

Repeat the above problem if $C_1 = 1.05C_2$.

Solution

In the sharing phase, we have the following equivalent circuit:



FigS10.4-02

$$v_{out}(i) = V_{C1}\frac{C_1}{C_1+C_2} + V_{C2}\frac{C_2}{C_1+C_2}$$

$$= \frac{1.05}{2.05}V_{C1} + \frac{1}{2.05}V_{C2}$$

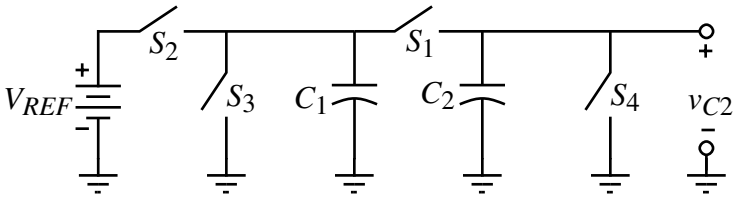
$$= 0.5122V_{C1} + 0.4878V_{C2}$$

Sharing Phase (i)	$V_{C1}(i)/V_{REF}$	$V_{C2}(i)/V_{REF}$	$V_{out}(i)/V_{REF}$
1	0	0	0
2	1	0	0.5112
3	0	0.5122	0.2498
4	1	0.2498	0.6340

Thus, at the end of the conversion, the output voltage is $0.6340V_{REF}$ rather than the ideal value of $0.6250V_{REF}$.

Problem 10.4-03

For the serial DAC shown, every time the switch S_2 opens, it causes the voltage on C_1 to be decreased by 10%. How many bits can this DAC convert before an error occurs assuming worst case conditions and letting V_{REF} = 1V? The analog output is taken across C_2.



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Solution

Worst case is for all 1's.

i	V_{C1}(ideal)	V_{C1}(act.)	V_{C2}(ideal)	V_{C2}(act.)	$\frac{V_{REF}}{2^{i+1}}$	$\lvert V_{C2}$(ideal) - V_{C2}(act.)$\rvert$	OK?
1	1	0.9	0.5	0.45	0.25	0.050	Yes
2	1	0.9	0.75	0.675	0.125	0.0750	Yes
3	1	0.9	0.875	0.7875	0.0625	0.0875	No

Error occurs at the third bit.

Note that the approach is to find the ideal value of V_{C2} at the ith bit and then find the range that V_{C2} could have which is $\pm V_{REF}/2^{i+1}$ and still not have an error. If the difference between the magnitude of the ideal value and actual value of V_{C2} exceeds $V_{REF}/2^{i+1}$ then an error will occur.

Problem 10.4-04

For the serial, pipeline DAC of Fig. 10.4-3 find the ideal analog output voltage if V_{REF} = 1V and the input is 10100110 from the *MSB* to the *LSB*. If the attenuation factors of 0.5 become 0.55, what is the analog output for this case?

Solution

Ignoring the delay terms,the output of Fig. 10.4-3 can be written as,

$$\frac{V_{out}}{V_{REF}} = b_0 + \frac{b_1}{2} + \frac{b_2}{4} + \frac{b_3}{8} + \frac{b_4}{16} + \frac{b_5}{32} + \frac{b_6}{64} + \frac{b_7}{128}$$

For 10100110 we get,

$$\frac{V_{out}}{V_{REF}}(\text{ideal}) = 1 - \frac{1}{2} + \frac{1}{4} - \frac{1}{8} - \frac{1}{16} + \frac{1}{32} + \frac{1}{64} - \frac{1}{128}$$

$$= \frac{128}{128} - \frac{64}{128} + \frac{32}{128} - \frac{16}{128} - \frac{8}{128} + \frac{4}{128} + \frac{2}{128} - \frac{1}{128} = \frac{77}{128} = 0.60156$$

If the attenuation factor is k = 0.55, the output can be re-expressed as,

$$\frac{V_{out}}{V_{REF}}(\text{actual}) = kb_0 + k^2b_1 + k^3b_2 + k^4b_3 + k^5b_4 + k^6b_5 + k^7b_6 + 8^8b_7$$

$$= +0.55 - 0.3025 + 0.1664 - 0.0915 - 0.0503 + 0.0277 + 0.0152 - 0.00837$$

$$= 0.3066$$

Problem 10.4-05

Give an implementation of the pipeline DAC of Fig. 10.4-3 using two-phase, switched capacitor circuits. Give a complete schematic with the capacitor ratios and switch phasing identified.

Solution

All of the stages can be represented by the following block diagram.

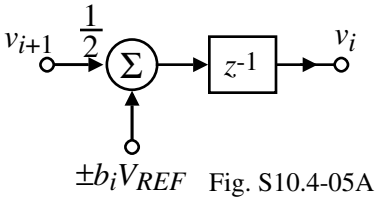
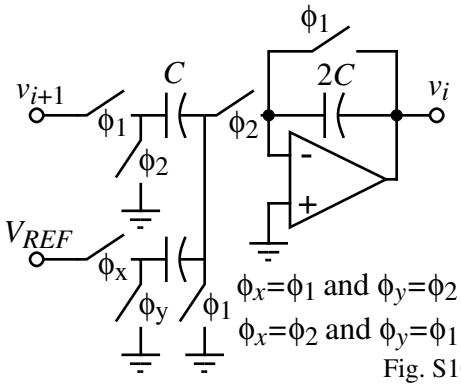


Fig. S10.4-05A

$$v_i = (0.5v_{i+1} \pm b_i V_{REF})z^{-1}$$

which is a summing sample and hold with weighted inputs. A possible switched-capacitor realization of the *i*-th stage (and all stages) is shown below.

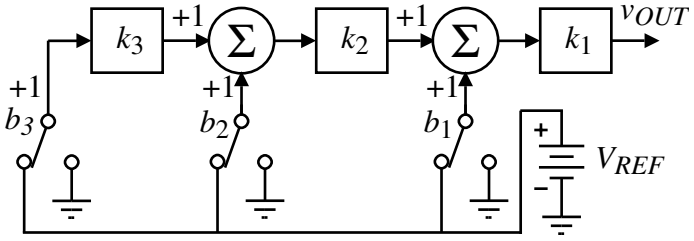


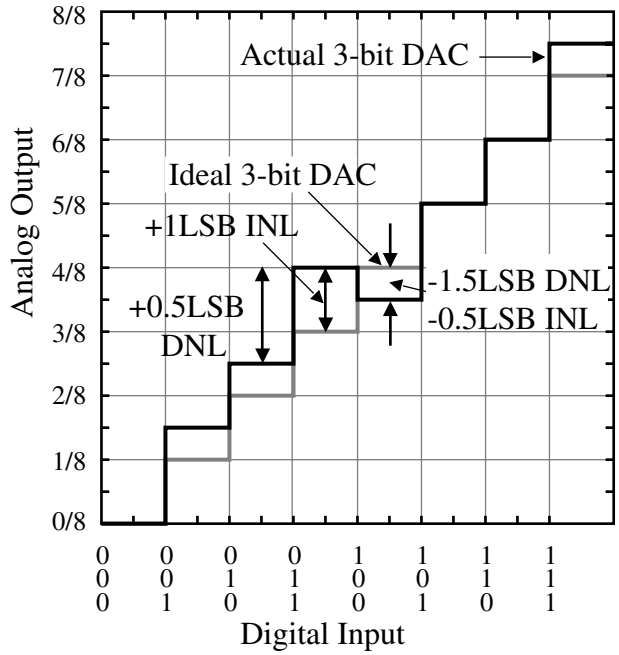
$\phi_x=\phi_1$ and $\phi_y=\phi_2$ if b_i=1
$\phi_x=\phi_2$ and $\phi_y=\phi_1$ if b_i=0

Fig. S10.4-5B

Problem 10.4-06

A pipeline DAC is shown. If k_1 = 7/16, k_2 = 5/7, and k_3 = 3/5 write an expression for v_{OUT} in terms of b_i (i = 1, 2, 3) and V_{REF}. Plot the input-output characteristic on the curve shown below and find the largest ±INL and largest ±DNL. Is the DAC monotonic or not?





Digital Word	v_{OUT}
000	0/16
001	3/16
010	5/16
011	8/16
100	7/16
101	10/16
110	12/16
111	15/16

Solution

The output can be written as

$$v_{OUT} = k_1(b_1+k_2(b_2+k_3b_3))V_{REF} = [k_1b_1 + k_1k_2b_2 + k_1k_2k_3b_3]V_{REF}$$

Using the values given gives

$$v_{OUT} = \left[\left(\frac{7}{16}\right)b_1 + \left(\frac{7}{16}\right)\left(\frac{5}{7}\right)b_2 + \left(\frac{7}{16}\right)\left(\frac{5}{7}\right)\left(\frac{3}{5}\right)b_3\right]V_{REF} = \left[\frac{7}{16}b_1 + \frac{5}{16}b_2 + \frac{3}{16}b_3\right]V_{REF}$$

The values for v_{OUT} for this DAC are shown beside the plot and have been plotted on the output-input characteristic curve. A summary of the performance is given below.

INL: +1LSB, -0.5LSB DNL: +0.5LSB, -1.5LSB DAC is nonmonotonic

Problem 10.4-07

A pipeline digital-analog converter is shown. When b_i is 1, the switch is connected to V_{REF}, otherwise it is connected to ground. Two of the 0.5 gains on the summing junctions are in error. Carefully sketch the resulting digital-analog transfer characteristic on the plot on the next page and identify the INL with respect to the infinite resolution characteristic shown and DNL. The INL and DNL should be measured on the analog axis.

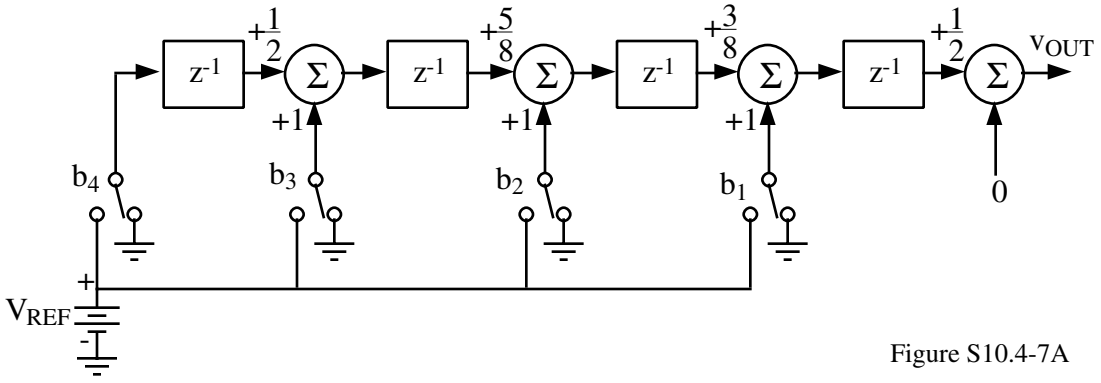


Figure S10.4-7A

Solution

Ignoring the delay terms, we can write the output voltage as,

$$\frac{v_{OUT}}{V_{REF}} = \left(\left(\left(\frac{b_4}{2} + b_3\right)\frac{5}{8} + b_2\right)\frac{3}{8} + b_1\right)\frac{1}{2} = \frac{1}{2}b_1 + \frac{3}{16}b_2 + \frac{30}{256}b_3 + \frac{15}{256}b_3$$

$$= \frac{128}{256}b_1 + \frac{48}{256}b_2 + \frac{30}{256}b_3 + \frac{15}{256}b_3$$

The performance is summarized in the table below (a plot can be made from the table).

B0	B1	B2	B3	Ideal	Actual	Ideal DNL	Actual DNL	Ideal INL	Actual INL
0	0	0	0	0.00000	0.00000	-	-	0.00000	0.00000
0	0	0	1	0.06250	0.05859	0.00000	-0.06250	0.00000	-0.06250
0	0	1	0	0.12500	0.11719	0.00000	-0.06250	0.00000	-0.12500
0	0	1	1	0.18750	0.17578	0.00000	-0.06250	0.00000	-0.18750
0	1	0	0	0.25000	0.18750	0.00000	-0.81250	0.00000	-1.00000
0	1	0	1	0.31250	0.24609	0.00000	-0.06250	0.00000	-1.06250
0	1	1	0	0.37500	0.30469	0.00000	-0.06250	0.00000	-1.12500
0	1	1	1	0.43750	0.36328	0.00000	-0.06250	0.00000	-1.18750
1	0	0	0	0.50000	0.50000	0.00000	1.18750	0.00000	0.00000
1	0	0	1	0.56250	0.55859	0.00000	-0.06250	0.00000	-0.06250
1	0	1	0	0.62500	0.61719	0.00000	-0.06250	0.00000	-0.12500
1	0	1	1	0.68750	0.67578	0.00000	-0.06250	0.00000	-0.18750
1	1	0	0	0.75000	0.68750	0.00000	-0.81250	0.00000	-1.00000
1	1	0	1	0.81250	0.74609	0.00000	-0.06250	0.00000	-1.06250
1	1	1	0	0.87500	0.80469	0.00000	-0.06250	0.00000	-1.12500
1	1	1	1	0.93750	0.86328	0.00000	-0.06250	0.00000	-1.18750

$\therefore$ $INL = +0\ LSBs,\ -1.1875 LSBs$ and $DNL = +1.1875 LSBs,\ -0.8125 LSBs$

Problem 10.4-08

Show how Eq. (10.4-2) can be derived from Eq. (10.4-1). Also show in the block diagram of Fig. 10.4-4 how the initial zeroing of the output can be accomplished.

Solution

Eq. (10.4-1) can be written as

$$V_{out} = \sum_{i=1}^{N} \frac{b_{i-1} z^{-i}}{2^{i-1}} = \sum_{i=1}^{N} \frac{b_{i-1} z^{-i}}{2^{i-1}} \frac{z}{z} = \frac{1}{z} \sum_{i=1}^{N} \frac{b_{i-1}}{2^{i-1} z^{i-1}} = \frac{1}{z} \sum_{i=1}^{N} \frac{b_{i-1}}{2^{i-1} z^{i-1}}$$

$$= \frac{1}{z} \sum_{i=0}^{N} \frac{b_i}{2^i z^i} = \frac{b_i}{z} \sum_{i=0}^{N} \frac{1}{2^i z^i}$$

where all b_i have assumed to be identical as stated in the text.

The summation can be recognized as a geometric series (assuming $N \to \infty$) to give

$$V_{out} = \frac{b_i}{z} \left[\frac{1}{1 - \frac{1}{2z}} \right] = \frac{b_i z^{-1}}{1 - 0.5 z^{-1}}$$

The output can initially be zeroed by adding a third switch to ground at the summing junction. The S/H will sample the 0V and produce $V_{out} = 0$.

Problem 10.4-09

Assume that the amplifier with a gain of 0.5 in Fig. 10.4-4 has a gain error of ΔA. What is the maximum value ΔA can be in Example 10.4-2 without causing the conversion to be in error?

Solution

Let the amplifier gain be A. Therefore, we can write the output in general as follows.

Bit from LSB to MSB	V_{out}
1	1
0	A-1
0	$A(A\text{-}1) + 1 = A^2 - A - 1$
1	$A[A(A\text{-}1) - 1] + 1 = A^3 - A^2 - A + 1$
1	$A\{A[A(A\text{-}1) - 1] + 1\} + 1 = A^4 - A^3 - A^2 + A + 1$

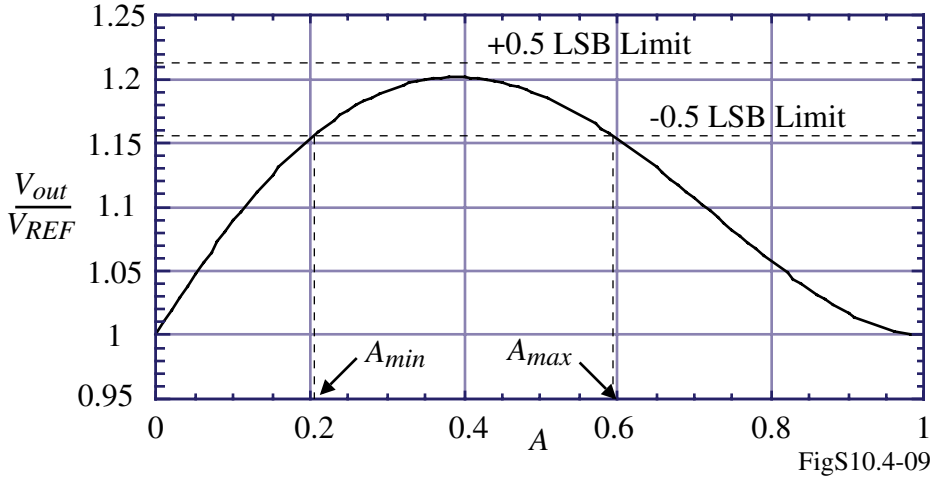
The ideal output is $V_{out} = \frac{19}{16} \pm 0.5LSB$ $\qquad LSB = \frac{2V_{REF}}{2^6} = \frac{V_{REF}}{2^5} = \frac{V_{REF}}{32}$

Assume V_{REF} = 1V, therefore

$$A^4 - A^3 - A^2 + A + 1 \le \frac{19}{16} \pm \frac{1}{32} = \frac{38}{32} \pm \frac{1}{32}$$

$\therefore$ The ideal output is 1.18750 and must be between 1.15625 and 1.21875.

Below is a plot of the output as a function of A.



FigS10.4-09

From this plot, we see that A must lie between 0.205 and 0.590 in order to avoid a $\pm 0.5LSB$ error.

$\therefore$ $\boxed{0.205 \le A \le 0.590}$

Problem 10.4-10

Repeat Example 10.4-2 for the digital word 10101.

Solution

Let the amplifier gain be A. Therefore, we can write the output in general as follows.

Bit from LSB to MSB	V_{out}
1	1
0	A-1
1	$A(A\text{-}1) + 1 = A^2 - A + 1$
0	$A[A(A\text{-}1) + 1] - 1 = A^3 - A^2 + A - 1$
1	$A\{A[A(A\text{-}1) + 1] - 1\} + 1 = A^4 - A^3 + A^2 - A + 1$

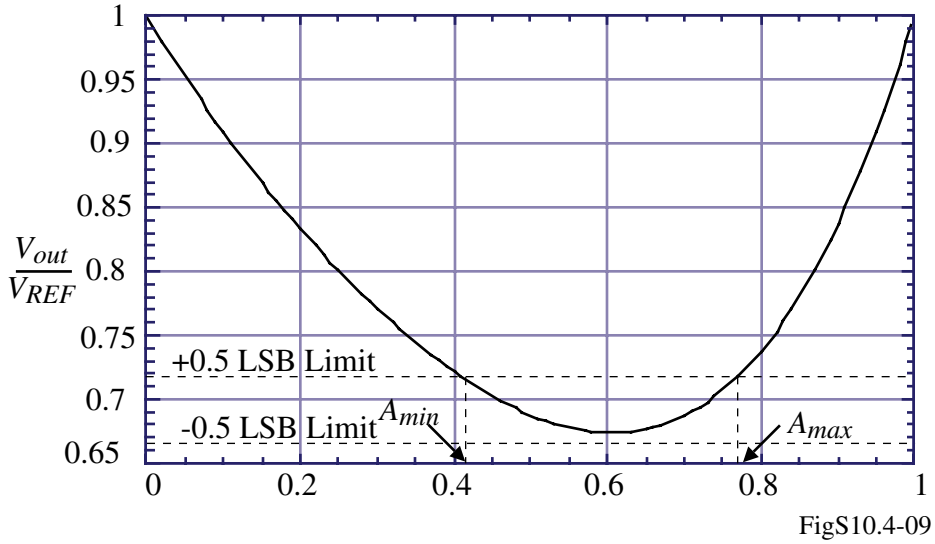
The ideal output is $V_{out} = \frac{11}{16} \pm 0.5LSB$ $\qquad LSB = \frac{2V_{REF}}{2^6} = \frac{V_{REF}}{2^5} = \frac{V_{REF}}{32}$

Assume $V_{REF} = 1$V, therefore

$$A^4 - A^3 - A^2 + A + 1 \le \frac{12}{16} \pm \frac{1}{32} = \frac{22}{32} \pm \frac{1}{32}$$

$\therefore$ The ideal output is 0.6875 and must be between 0.65625 and 0.71875.

Below is a plot of the output as a function of A.



FigS10.4-09

From this plot, we see that A must lie between 0.41 and 0.77 in order to avoid a $\pm 0.5LSB$ error.

$\therefore$ $\boxed{0.41 \le A \le 0.77}$

Problem 10.4-11

Assume that the iterative algorithmic DAC of Fig. 10.4-4 is to convert the digital word 11001. If the gain of the 0.5 amplifier is 0.7, at which bit conversion is an error made?

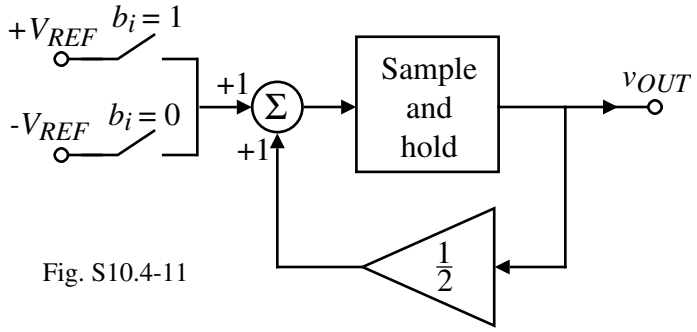


Fig. S10.4-11

Solution

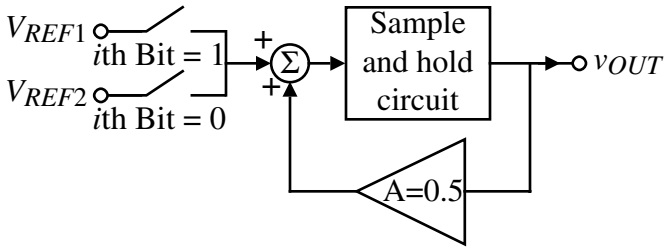
Conversion No.	Bit Converted	Ideal Result	Max. Ideal	Min. Ideal	Result for Gain = 0.7
1	1(LSB)	1	1.5	0.5	1 (OK)
2	0	-(1/2)	-0.25	-0.75	-0.30 (OK)
3	0	-(5/4)	-1.1250	-1.375	-1.210 (OK)
4	1	(3/8)	0.4375	0.3125	0.1530 (Error)
5	1 (MSB)	(19/16)	0.9062	0.8437	-

The max. and min. ideal are found by taking the ideal result and adding and substracting half of the ideal bit for that conversion number.

We note from the table that the error occurs in the 4th bit conversion.

Problem 10.4-12

An iterative, algorithmic DAC is shown in Fig. P10.4-12. Assume that the digital word to be converted is 10011. If V_{REF1} =0.9V_{REF} and V_{REF2} = -0.8V_{REF}, at which bit does an error occur in the conversion of the digital word to an analog output?



Solution

Ideally, the output of the i-th stage should be,

$$v_{OUT}(i) = 0.5\ v_{OUT}(i\text{-}1) \pm b_i V_{REF}$$

The i-th *LSB* is given as $\dfrac{V_{REF}}{2^{i-1}}$.

In this problem, the output of i-th stage is given as,

$$v_{OUT}(i) = 0.5\ v_{OUT}(i\text{-}1) + 0.9V_{REF} \quad \text{if } b_i = 1$$

and

$$v_{OUT}(i) = 0.5\ v_{OUT}(i\text{-}1) - 0.8V_{REF} \quad \text{if } b_i = 0$$

The performance is summarized in the following table where $v_{OUT}(i)$ is normalized to V_{REF}.

Conversion No.	0.5 *LSB*	Bit Converted	$v_{OUT}(i)$ Ideal	Max. Ideal $v_{OUT}(i)$	Min. Ideal $v_{OUT}(i)$	Actual $v_{OUT}(i)$
1	0.5	1	1	1.5	0.5	0.9
2	0.25	1	1.5	1.75	1.25	1.35
3	0.125	0	-0.25	-0.125	-0.375	-0.125
4	0.0625	0	-1.125	-1.0625	-1.1875	-0.8625
5	0.03125	1	0.4375	0.46875	0.40625	0.46875

An error occurs in the 4th bit conversion since it lies outside the maximum-minimum ideal $v_{OUT}(i)$. Note the 5th bit is okay.

Problem 10.5-01

Plot the transfer characteristic of a 3-bit ADC that has the largest possible differential nonlinearity when the integral nonlinearity is limited to ±1*LSB*. What is the maximum value of the differential nonlinearity for this case?)

Solution

A plot is given below showing the upper and lower limits for ±1 LSB INL. The dark line on the plot shows part of the ADC characteristics that illustrates that the maximum DNL is ±2 LSB.

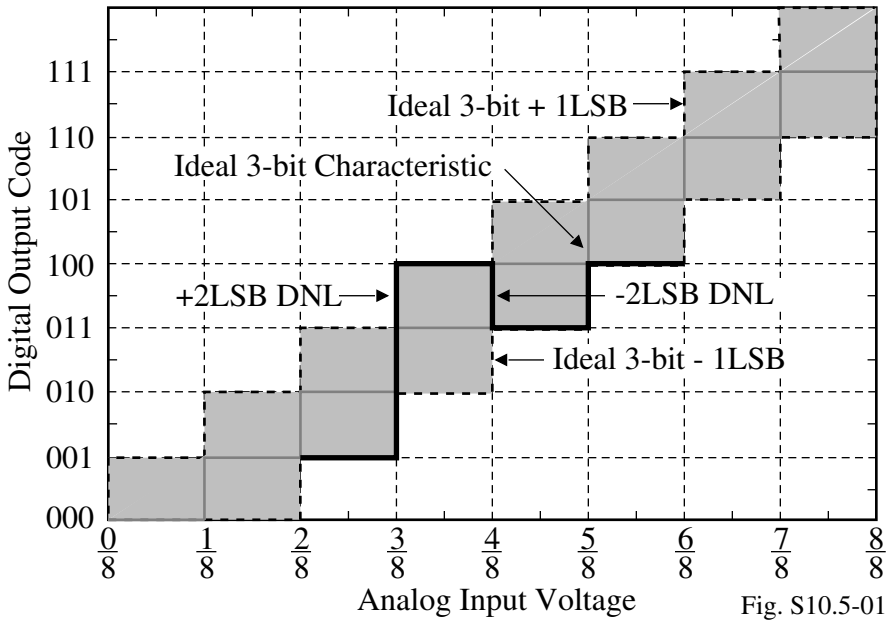


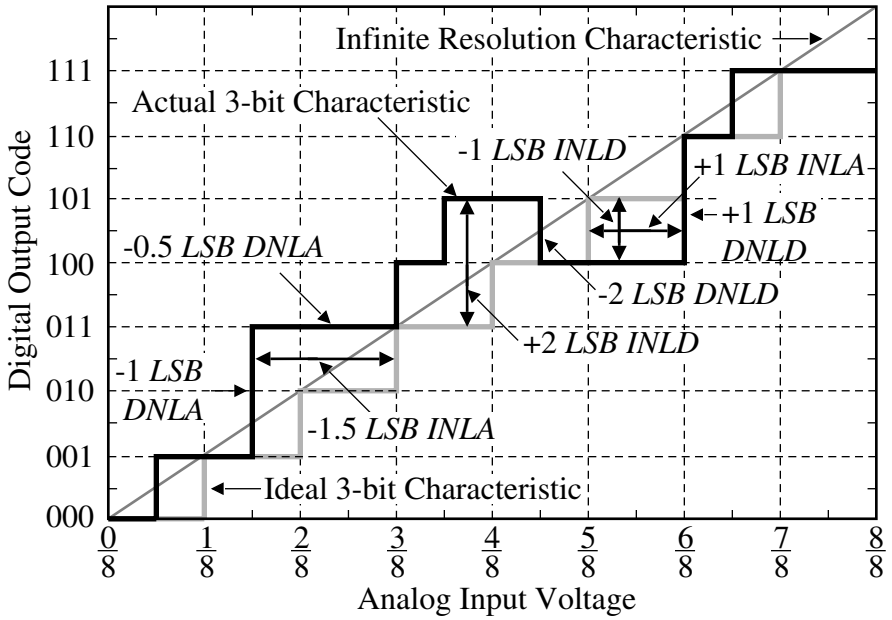
Fig. S10.5-01

Problem 10.5-2

(a.) Find the ±*INL* and ±*DNL* for the 3-bit ADC shown where the *INL* and *DNL* is referenced to the analog input voltage. (Use the terminology: *INLA* and *DNLA*.)

(b.) Find the ±*INL* and ±*DNL* for the 3-bit ADC shown where the *INL* and *DNL* is referenced to the digital output code. (Use the terminology: *INLD* and *DNLD*.)

(c.) Is this ADC monotonic or not?



Solutions

(a.) Refer to the characteristics above:

$+INLA = 1LSB$ $-INLA = -1.5LSB$

$+DNLA = +0.5LSB$ $-DNLA = -1LSB$

(b.) Refer to the characteristics above:

$+INLD = 2LSB$ $-INLD = -1LSB$

$+DNLD = +1LSB$ $-DNLD = -2LSB$

(c.) This ADC is not monotonic.

Problem 10.5-03

Assume that the step response of a sample-and-hold circuit is

$$v_{OUT}(t) = V_I(1 - e^{-t\text{Æ}BW})$$

where V_I is the magnitude of the input step to the sample-and-hold and BW is the bandwidth of the sample-and-hold circuit in radians/sec. and is equal to 2πMradians/sec. Assume a worst case analysis and find the maximum number of bits this sample-and-hold circuit can resolve if the sampling frequency is 1MHz. (Assume that the sample-and-hold circuit has the entire period to acquire the sample.)

Solution

To avoid an error, the value of $v_{OUT}(t)$ should be within ±0.5*LSB* of V_I. Since v_{OUT} is always less than V_I let us state the requirements as

$$V_I - v_{OUT}(T) \le \frac{V_{REF}}{2^{N+1}}$$

$$\therefore\ V_I - V_I(1-e^{-T\cdot BW}) \le \frac{V_{REF}}{2^{N+1}} \ \rightarrow\ V_I e^{-T\cdot BW} \le \frac{V_{REF}}{2^{N+1}} \ \rightarrow\ 2^{N+1} \le \frac{V_I}{V_{REF}} e^{T\cdot BW}$$

The worst case value is when $V_I = V_{REF}$. Thus,

$$2^{N+1} \le e^{2\pi} = 535.49 \quad \rightarrow \quad 2^N \le \frac{535.49}{2} = 267.74$$

$$\therefore\ \boxed{N = 8}$$

Problem 10.5-04

If the aperture jitter of the clock in an ADC is 200ps and the input signal is a 1MHz sinusoid with a peak-to-peak value of V_{REF}, what is the number of bits that this ADC can resolve?

Solution

Eq. (10.8-1) gives $\Delta t \le \frac{V_{REF}}{2^{N+1}} \frac{2}{2\pi f V_{REF}} = \frac{1}{2^{N+1}\pi f} = 200\text{ps}$

$$2^N = \frac{1}{2\cdot 200\text{ps}\cdot \pi\text{MHz}} = \frac{10^6}{400\pi} = 756$$

$$ln(2^N) = ln(756) \qquad \rightarrow \qquad N = \frac{ln(756)}{ln(2)} = 9.63$$

$\therefore$ $\underline{\underline{N = 9\text{bits}}}$

Problem 10.6-01

What is the conversion time in clock periods if the input to Fig. 10.6-2 is 0.25 V_{REF}? Repeat if $v_{in}{}^{*} = 0.7V_{REF}$.

Solution

$v_{in}{}^{*} = 0.25V_{REF}$:

$$N_{out} = N_{REF}\text{x}0.25 = 0.25N_{REF}$$

$\therefore$ Clock periods = $N_{REF} + 0.25N_{REF} = \underline{\underline{1.25N_{REF}}}$

$v_{in}{}^{*} = 0.7V_{REF}$:

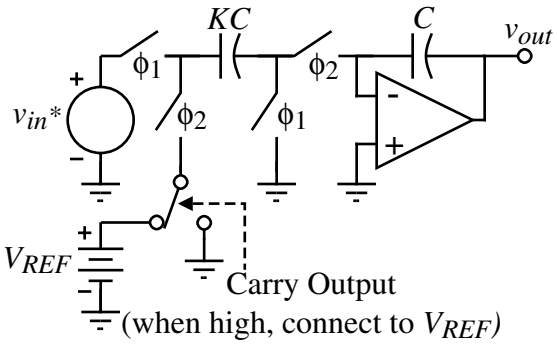
$$N_{out} = N_{REF}\text{x}0.7 = 0.7N_{REF}$$

$\therefore$ Clock periods = $N_{REF} + 0.7N_{REF} = \underline{\underline{1.7N_{REF}}}$

Problem 10.6-02

Give a switched capacitor implementation of the positive integrator and the connection of the input and reference voltage to the integrator via switches 1 and 2 using a two-phase clock.

Solution



FS10.6-02

From Chapter 9, it can be shown that,

$$v_{out}(t) \approx K\int v_{in}{}^{*}\, dt \quad \text{or} \quad -K\int V_{REF}\, dt$$

depending on the carrier output.

Problem 10.7-01

If the sampled, analog input applied to an 8-bit successive-approximation converter is $0.7V_{REF}$, find the output digital word.

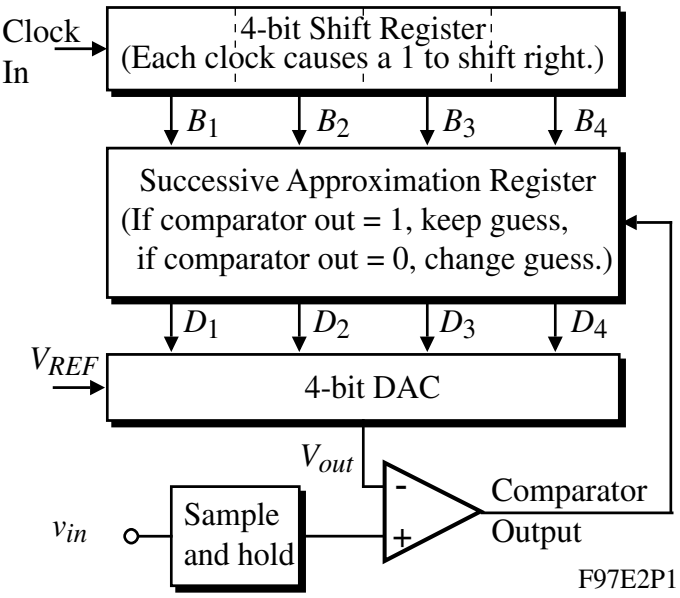
Solution

Bit	Trial Digital Word $b_0b_1b_2b_3b_4b_5b_6b_7$	$DV_{REF} = \left(\frac{b_0}{2}+\frac{b_1}{4}+\frac{b_2}{8}+\frac{b_3}{16}+\frac{b_4}{32}+\frac{b_5}{64}+\frac{b_6}{128}+\frac{b_7}{256}\right)V_{REF}$	$0.7V_{REF} > DV_{REF}$?	Decoded Bit
1	1 0 0 0 0 0 0 0	$0.5V_{REF}$	Yes	1
2	1 1 0 0 0 0 0 0	$0.75V_{REF}$	No	0
3	1 0 1 0 0 0 0 0	$0.625V_{REF}$	Yes	1
4	1 0 1 1 0 0 0 0	$0.6875V_{REF}$	Yes	1
5	1 0 1 1 1 0 0 0	$0.71875V_{REF}$	No	0
6	1 0 1 1 0 1 0 0	$0.703125V_{REF}$	No	0
7	1 0 1 1 0 0 1 0	$0.6953125V_{REF}$	Yes	1
8	1 0 1 1 0 0 1 1	$0.69921875V_{REF}$	Yes	1

The digital word is 1 0 1 1 0 0 1 1

Problem 10.7-02

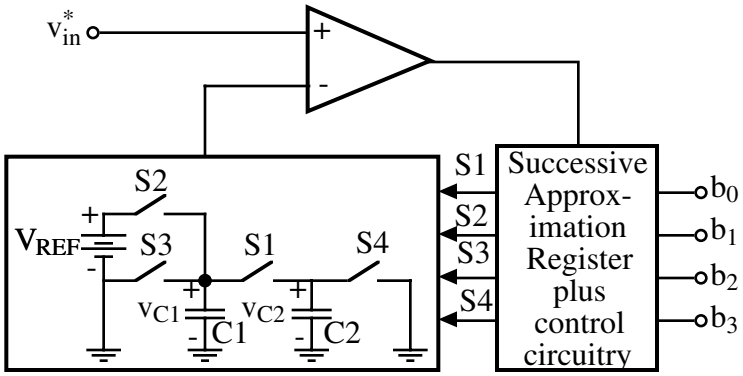
A 4-bit, successive approximation ADC is shown. Assume that V_{REF} = 5V. Fill in the table below when v_{in} = 3V.



Clock Period	$B_1B_2B_3B_4$	Guessed $D_1D_2D_3D_4$	V_{out}	Comparator Output	Actual $D_1D_2D_3D_4$
1	1 0 0 0	1 0 0 0	2.5V	1	1 0 0 0
2	0 1 0 0	1 1 0 0	3.75V	0	1 0 0 0
3	0 0 1 0	1 0 1 0	3.125V	0	1 0 0 0
4	0 0 0 1	1 0 0 1	2.8125V	1	1 0 0 1

Problem 10.7-03

For the successive approximation ADC shown in Fig. 10.7-7, sketch the voltage across capacitor C_1 (v_{C1}) and C_2 (v_{C2}) of Fig. 10.4-1 if the sampled analog input voltage is $0.6V_{REF}$. Assume that $S2$ and $S3$ closes in one clock period and $S1$ closes in the following clock period. Also, assume that one clock period exists between each successive iteration. What is the digital word out?



Actual digital word is 1001.

i	Guess	v_{Guess}	Actual
0	1	0.5	1
1	11	0.75	1.0
2	101	0.625	100
3	1001	0.5625	1001

Solution

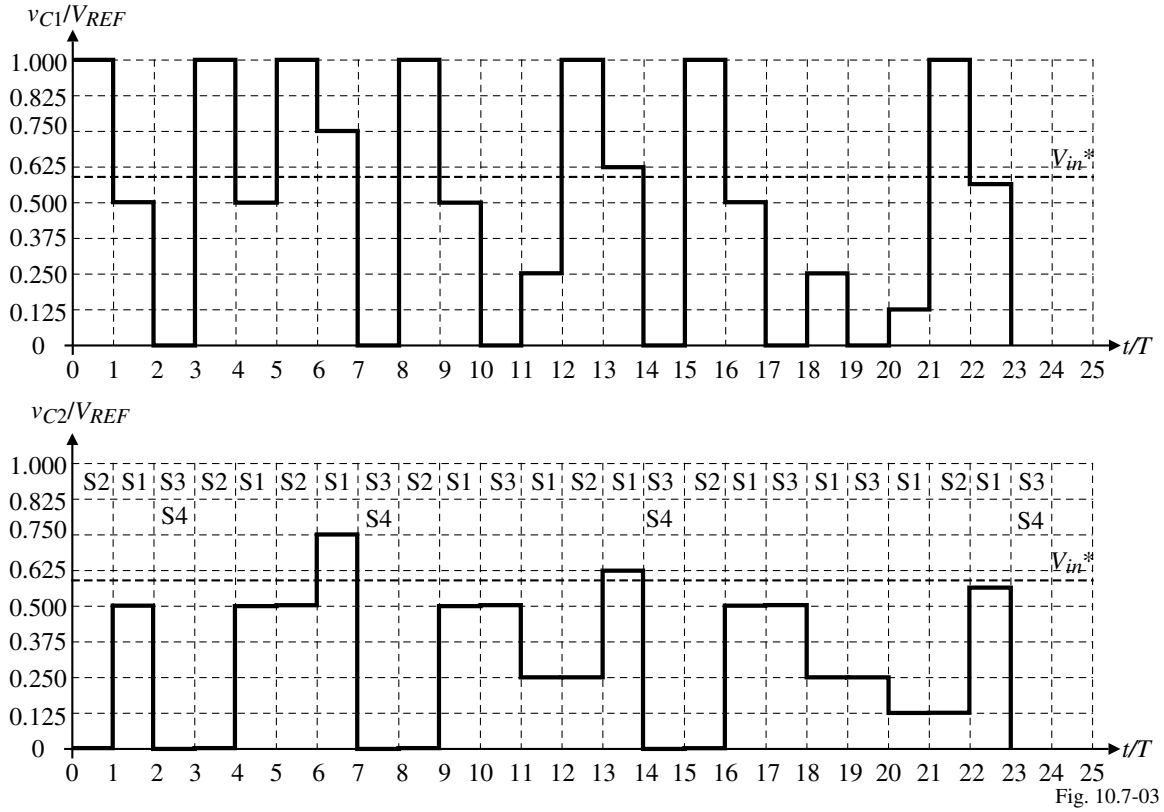


Fig. 10.7-03

Problem 10.7-04

Assume that the input of Example 10.7-1 is $0.8V_{REF}$ and find the digital output word to 6 bits.

Solution

b_0: $V_{in}(0) = 0.8V_{REF}$ → $b_0 = 1$

b_1: $V_{in}(1) = 2(0.8V_{REF}) - V_{REF} = +0.6V_{REF}$ → $b_1 = 1$

b_2: $V_{in}(2) = 2(0.6V_{REF}) - V_{REF} = +0.2V_{REF}$ → $b_2 = 1$

b_3: $V_{in}(3) = 2(0.2V_{REF}) - V_{REF} = -0.6V_{REF}$ → $b_3 = 0$

b_4: $V_{in}(4) = 2(-0.6V_{REF}) + V_{REF} = -0.2V_{REF}$ → $b_4 = 0$

b_5: $V_{in}(5) = 2(-0.2V_{REF}) + V_{REF} = +0.6V_{REF}$ → $b_5 = 1$

$\therefore$ Digital output word = 1 1 1 0 0 1

Problem 10.7-05

Assume that the input of Example 10.7-1 is $0.3215V_{REF}$ and find the digital output word to 8 bits.

Solution

b_0: $V_{in}(0) = 0.3215V_{REF}$ → $b_0 = 1$

b_1: $V_{in}(1) = 2(0.3125V_{REF}) - V_{REF} = -0.357V_{REF}$ → $b_1 = 0$

b_2: $V_{in}(2) = 2(-0.357V_{REF}) + V_{REF} = +0.286V_{REF}$ → $b_2 = 1$

b_3: $V_{in}(3) = 2(0.286V_{REF}) - V_{REF} = -0.428V_{REF}$ → $b_3 = 0$

b_4: $V_{in}(4) = 2(-0.428V_{REF}) + V_{REF} = +0.144V_{REF}$ → $b_4 = 1$

b_5: $V_{in}(5) = 2(0.144V_{REF}) - V_{REF} = -0.712V_{REF}$ → $b_5 = 0$

b_6: $V_{in}(6) = 2(-0.712V_{REF}) + V_{REF} = -0.424V_{REF}$ → $b_4 = 0$

b_7: $V_{in}(7) = 2(-0.424V_{REF}) + V_{REF} = +0.152V_{REF}$ → $b_4 = 1$

$\therefore$ Digital output word = 1 0 1 0 1 0 0 1

Problem 10.7-06

Repeat Example 10.7-1 for 8 bits if the gain of two amplifiers actually have a gain of 2.1.

Solution

$$v_{in}^* = \frac{1.50}{5.00} V_{REF} = 0.3V_{REF}$$

b_0: $V_{in}(0) = 0.3V_{REF} \rightarrow b_0 = 1$

b_1: $V_{in}(1) = 2.1(0.3V_{REF}) - V_{REF} = -0.37V_{REF} \rightarrow b_1 = 0$

b_2: $V_{in}(2) = 2.1(-0.37V_{REF}) + V_{REF} = +0.223V_{REF} \rightarrow b_2 = 1$

b_3: $V_{in}(3) = 2.1(+0.223V_{REF}) - V_{REF} = -0.5317V_{REF} \rightarrow b_3 = 0$

b_4: $V_{in}(4) = 2.1(-0.5317V_{REF}) + V_{REF} = -0.0634V_{REF} \rightarrow b_4 = 0$

b_5: $V_{in}(5) = 2.1(-0.0634V_{REF}) + V_{REF} = +0.86686V_{REF} \rightarrow b_5 = 1$

b_6: $V_{in}(6) = 2.1(+0.86686V_{REF}) - V_{REF} = +0.820406V_{REF} \rightarrow b_6 = 1$

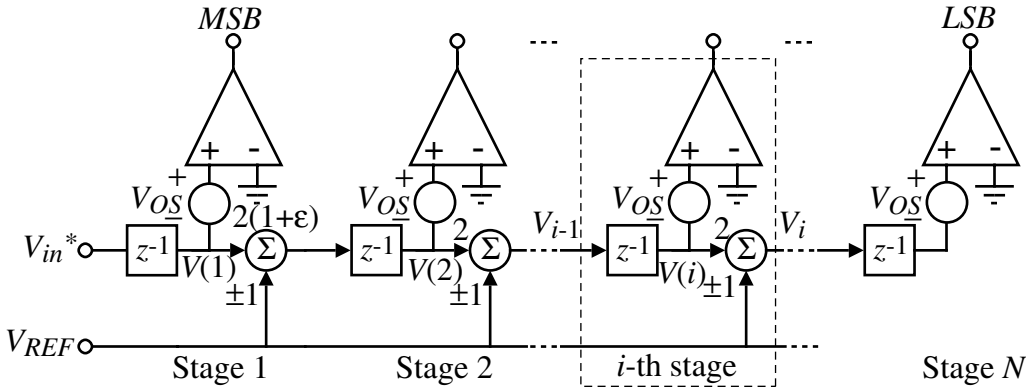
b_7: $V_{in}(7) = 2.1(+0.820406V_{REF}) - V_{REF} = +0.820406V_{REF} \rightarrow b_6 = 1$

The ideal digital word for Ex. 10.7-1 is 1 0 1 0 0 1 1 0

We see that the amplifier with a gain of 2.1 causes an error in the 8th bit.

Problem 10.7-07

Assume that $V_{in}^* = 0.7V_{REF}$ is applied to the pipeline algorithmic ADC of Fig. 10.7-9 with 5 stages. All elements of the converter are ideal except for the multiplier of 2 of the first stage, given as 2(1+ε). (a.) What is the smallest magnitude of ε that causes an error, assuming that the comparator offsets, V_{OS} , are all zero? (b.) Next, assume that the comparator offsets are all equal and nonzero. What is the smallest magnitude of the comparator offsets, V_{OS}, that causes an error, assuming that ε is zero?



Solution

Use the following table to solve this problem.

Stage No.	Bit Converted ($MSB \rightarrow LSB$)	$V(i)$	$V(i)$ with $\varepsilon(\imath)\neq 0$	$\varepsilon(i)^*$	$V(i)$ with $V_{OS}=0$
1	1	0.7	0.7	-	0.7
2	1	0.4	$1.4(1+\varepsilon)-1 = 0.4+1.4\varepsilon$	-0.286	0.4
3	0	-0.2	$2(0.4+1.4\varepsilon)-1 = -0.2+2.8\varepsilon$	0.0714	-0.2
4	1	0.6	$2(-0.2+2.8\varepsilon)+1 = 0.6+5.6\varepsilon$	-0.107	0.6
5	1	0.2	$2(0.6+5.6\varepsilon)-1 = 0.2+11.2\varepsilon$	-0.0178	0.2

*$\varepsilon(i)$ is calculated by setting $V(i)$ with $\varepsilon \neq 0$ to zero.

From the above table we get the following results:

$\therefore$ From the fifth column, we see that the minimum $|\varepsilon|$ is 0.0178

(b.) The minimum $V_{OS} = \pm 0.2$V.

Problem 10.7-08

The input to a pipeline algorithmic ADC is 1.5V. If the ADC is ideal and V_{REF} = 5V, find the digital output word up to 8 bits in order of *MSB* to *LSB*. If V_{REF} = 5.2 and the input is still 1.5V, at what bit does an error occur?

Solution

The iterative relationship of an algorithmic ADC is,

$v(i+1) = 2v(i) - b_i V_{REF}$ where $b_i = 1$ if $b_i =$ "1" and –1 if $b_i =$ "0".

Ideal case (V_{REF}=5V):

i	$v(i)$	b_i	$2v(i) - b_i V_{REF}$
1	1.5	1	3 - 5 = -2
2	-2	0	-4 + 5 = 1
3	1	1	2 – 5 = -3
4	-3	0	-6 + 5 = -1
5	-1	0	-2 + 5 = 3
6	3	1	6 – 5 = 1
7	1	1	2 – 5 = -3
8	-3	0	

Actual case (V_{REF}=5.2V):

i	$v(i)$	b_i	$2v(i) - b_i V_{REF}$
1	1.5	1	3 – 5.2 = -2.2
2	-2.2	0	-4.4 + 5.2 = 0.8
3	0.8	1	1.6 – 5.2 = -3.6
4	-3.6	0	-7.2 + 5.2 = -2.0
5	-2.0	0	-4 + 5.2 = 1.2
6	1.2	1	2.4 – 5.2 = -2.8
7	-2.8	0	-5.6 + 5.2 = -0.6
8	-0.6	0	

The error occurs at the 7th bit.

Problem 10.7-09

If $V_{in}{}^{*} = 0.1V_{REF}$, find the digital output of an ideal, 4-stage, algorithmic pipeline ADC. Repeat if the comparators of each stage have a dc voltage offset of 0.1V.

Solution

Ideal:

Stage i	V_{i-1}	$V_{i-1} > 0$?	Bit i
1	0.1	Yes	1
2	0.1x2-1.0 = -0.8	No	0
3	-0.8x2+1.0 = -0.6	No	0
4	-0.6x2+1.0 = -0.2	No	0

Offset = 0.1V:

$V_i = 2V_{i-1} - b_i V_{REF} + 0.1$

Stage i	V_{i-1}	$V_{i-1} > 0$?	Bit i
1	0.1	Yes	1
2	0.1x2-1.0+0.1 = -0.7	No	0
3	-0.7x2+1.0+0.1 = -0.3	No	0
4	-0.3x2+1.0+0.1 = +0.5	Yes	1

An error will occur in the 4th bit when $V_{in}{}^{*} = 0.1V_{REF}$ and the offset voltage is 0.1V.

Problem 10.7-10

Continue Example 10.7-3 out to the 10th bit and find the equivalent analog voltage.

Solution

$v_{in}{}^{*} = 0.8V_{REF}$

$V_a(0) = 2(0.8V_{REF}) = 1.6V_{REF}, \qquad 1.6\,V_{REF} > V_{REF} \quad \Rightarrow \quad b_0 = 1$

$V_a(1) = 2(1.6V_{REF} - V_{REF}) = 1.2V_{REF}, \qquad 1.2\,V_{REF} > V_{REF} \quad \Rightarrow \quad b_1 = 1$

$V_a(2) = 2(1.2V_{REF} - V_{REF}) = 0.4V_{REF}, \qquad 0.4\,V_{REF} < V_{REF} \quad \Rightarrow \quad b_2 = 0$

$V_a(3) = 2(0.4V_{REF} + 0) = 0.8V_{REF}, \qquad 0.8\,V_{REF} < V_{REF} \quad \Rightarrow \quad b_3 = 0$

(Note the ADC repeats at every 4 bits)

$V_a(4) = 2(0.8V_{REF} + 0) = 1.6V_{REF}, \qquad 1.6\,V_{REF} > V_{REF} \quad \Rightarrow \quad b_4 = 1$

$V_a(5) = 2(1.6V_{REF} - V_{REF}) = 1.2V_{REF}, \qquad 1.2\,V_{REF} > V_{REF} \quad \Rightarrow \quad b_5 = 1$

$V_a(6) = 2(1.2V_{REF} - V_{REF}) = 0.4V_{REF}, \qquad 0.4\,V_{REF} < V_{REF} \quad \Rightarrow \quad b_6 = 0$

$V_a(7) = 2(0.4V_{REF} + 0) = 0.8V_{REF}, \qquad 0.8\,V_{REF} < V_{REF} \quad \Rightarrow \quad b_7 = 0$

Repeats again.

$\therefore$ The digital output word is 1 1 0 0 1 1 0 0 1 1 0 0 ……..

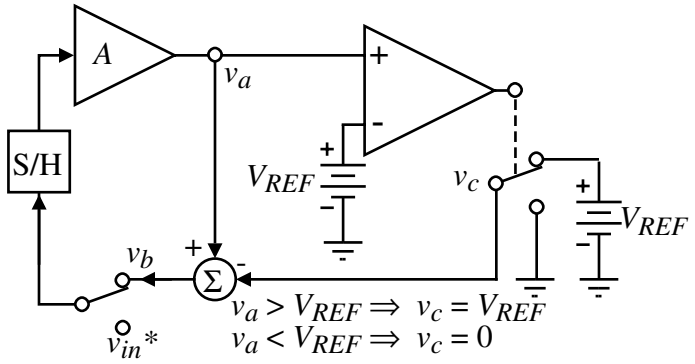
The analog equivalent is

$$V_{REF}\left(\frac{1}{2} + \frac{1}{4} + \frac{0}{8} + \frac{0}{16} + \frac{1}{32} + \frac{1}{64} + \frac{0}{128} + \frac{0}{256} + \frac{1}{512} + \frac{1}{1024} + \cdots\right)$$

$$= 0.79980469V_{REF}$$

Problem 10.7-11

Repeat Example 10.7-3 if the gain of two amplifier actually has a gain of 2.1.



Solution

(a.) A = 2.0. Assume V_{REF} = 1V.

i	$v_a(i)$	$v_a(i) > V_{REF}$?	b_i	$v_b(i)$
1	2(0.8)=1.6	Yes	1	0.6
2	2(0.6)=1.2	Yes	1	0.2
3	2(0.2)=0.4	No	0	0.4
4	2(0.4)=0.8	No	0	0.8
5	2(0.8)=1.6	Yes	1	0.6

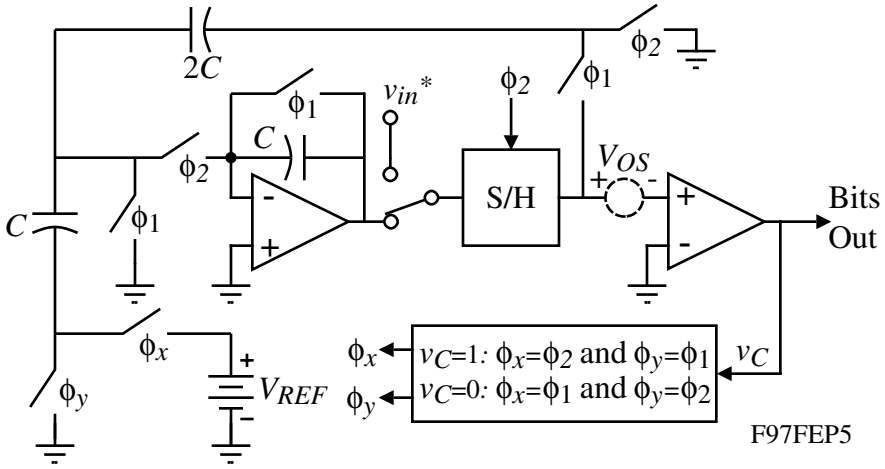
(b.) A = 2.1. Assume V_{REF} = 1V.

i	$v_a(i)$	$v_a(i) > V_{REF}$?	b_i	$v_b(i)$
1	2.1(0.8)=1.68	Yes	1	0.68
2	2.1(0.68)=1.428	Yes	1	0.428
3	2.1(0.428)=0.8988	No	0	0.8988
4	2.1(0.8988)=1.88748	Yes	1	0.88748
5	2.1(0.88748)=1.886371	Yes	1	0.886371

An error occurs in the 4th bit.

Problem 10.7-12

An algorithmic ADC is shown below where ϕ_1 and ϕ_2 are nonoverlapping clocks. Note that the conversion begins by connecting $v_{in}{}^*$ to the input of the sample and hold during a ϕ_2 phase. The actual conversion begins with the next phase period, ϕ_1. The output bit is taken at each successive ϕ_2 phase. (a.) What is the 8-bit digital output word if $v_{in}{}^* = 0.3V_{REF}$? (b.) What is the equivalent analog of the digital output word? (c.) What is the largest value of comparator offset, V_{OS}, before an error is caused in part (a.) if V_{REF} = 1V?



Solution

(a.)

Clock Period	Output of S/H (Normalized to V_{REF})	$v_C > 0$?	Digital Output
Start	0.3V	Yes	-
1	(0.3·2) - 1 = -0.4V	No	0
2	(-0.4·2) + 1 = 0.2V	Yes	1
3	(0.2·2) - 1 = -0.6V	No	0
4	(-0.6·2) + 1 = -0.2V	No	0
5	(-0.2·2) + 1 = 0.6V	Yes	1
6	(0.6·2) -1 = 0.2V	Yes	1
7	(0.2·2) - 1 = -0.6V	No	0
8	(-0.6·2) + 1 = -0.2V	No	0

(b.) $$V_{analog} = \left(\frac{1}{4} + \frac{1}{32} + \frac{1}{64}\right) V_{REF} = 0.296875 V_{REF}$$

(c.) In part (a.) the output of the S/H never got smaller than $\pm 0.2V_{REF} = \pm 0.2$V.

Problem 10.8-01

Why are only 2^N-1 comparators required for a N-bit flash A/D converter? Give a logic diagram for the digital decoding network of Fig. 10.8-1 which will provide the correct digital output word.

Solution

(See the solution for Problem 10.22 of the first edition)

Problem 10.8-02

What are the comparator outputs in order of the upper to lower if V^*_{in} is $0.6V_{REF}$ for the A/D converter of Fig. 10.8-1?

Solution

The comparator outputs in order from the upper to lower of Fig. 10.8-1 for $V^*_{in} = 0.6V_{REF}$ is

1 1 1 0 0 0 0.

Problem 10.8-03

Figure P10.8-3 shows a proposed implementation of the conventional 2-bit flash analog-to-digital converter (digital encoding circuitry not shown) shown on the left with the circuit on the right. Find the values of C_1, C_2, and C_3 in terms of C that will accomplish the function of the conventional 2-bit flash analog-to-digital. Compare the performance of the two approaches from the viewpoints of comparator offset, speed of conversion, and accuracy of conversion assuming a CMOS integrated circuit implementation.

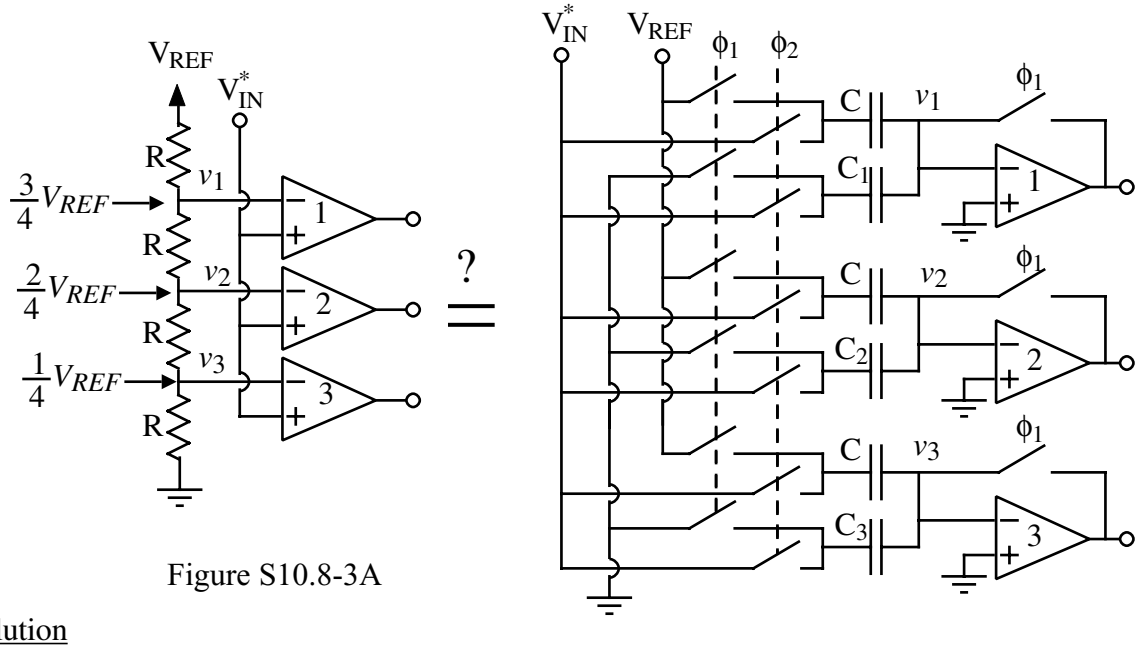


Figure S10.8-3A

Solution

Operation:

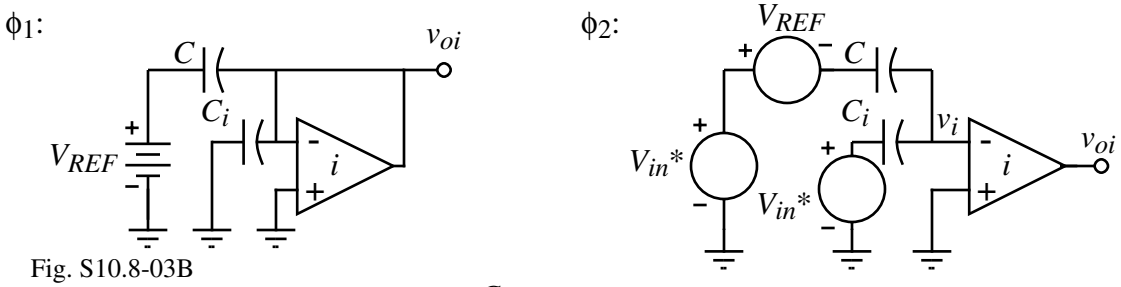


Fig. S10.8-03B

$$v_i(\phi_2) = (V_{in}^* - V_{REF})\left(\frac{C}{C+C_i}\right) + \left(\frac{C_i}{C+C_i}\right)V_{in}^* = V_{in}^* - V_{REF}\left(\frac{C}{C+C_i}\right)$$

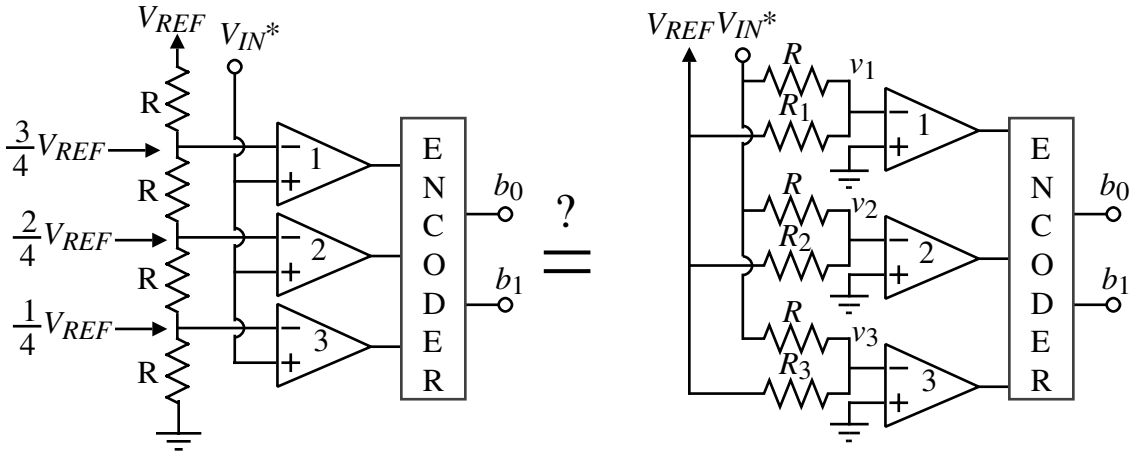
For the conventional flash ADC, $v_i = V_{in}^* - \frac{2^N - i}{2^N} V_{REF}$. For $N = 2$, we get

$$\therefore \frac{2^N - i}{2^N} = \frac{C}{C+C_i} \rightarrow C_i = \left(\frac{i}{2^N - i}\right)C$$ For $N = 2$, we get $C_1 = C/3$, $C_2 = C$, and $C_3 = 3C$

ADC	Comp. Offset	Conv. Speed	Accuracy	Other Aspects
Conv. Flash ADC	$\leq \pm 0.5LSB$	Fast	Poor	Equal R's
Proposed ADC	Autozeroed	Faster, comp. is simpler	Better	Unequal C's, No CMRR problems

Problem 10.8-04

Two versions of a 2-bit, flash A-D converter are shown in Fig. P10.8-5. Design R_1, R_2, and R_3 to make the right-hand version be equivalent to the left-hand version of the 2-bit flash A-D converter. Compare the performance advantages and disadvantages between the two A-D converters.



Conventional Flash ADC Proposed Flash ADC

Figure S10.8-04

Solution

For the proposed ADC, the comparators must switch at $V_{in}* = 0.75V_{REF}$, $0.5V_{REF}$ and $0.25V_{REF}$ for comparators, 1,2, and 3, respectively.

$$\therefore\ v_1 = \left(\frac{R_1}{R+R_1}\right)V_{in}* - \left(\frac{R}{R+R_1}\right)V_{REF} = 0 \quad \rightarrow \quad V_{in}* = \left(\frac{R}{R_1}\right)V_{REF} \quad \rightarrow \quad R_1 = (4/3)R$$

$$v_2 = \left(\frac{R_2}{R+R_2}\right)V_{in}* - \left(\frac{R}{R+R_1}\right)V_{REF} = 0 \quad \rightarrow \quad V_{in}* = \left(\frac{R}{R_2}\right)V_{REF} \quad \rightarrow \quad R_2 = 2R$$

and

$$v_3 = \left(\frac{R_3}{R+R_3}\right)V_{in}* - \left(\frac{R}{R+R_3}\right)V_{REF} = 0 \quad \rightarrow \quad V_{in}* = \left(\frac{R}{R_3}\right)V_{REF} \quad \rightarrow \quad R_3 = 4R$$

Comparison:

	Conventional Flash ADC	Proposed Flash ADC
Advantages	Less resistor area Guaranteed monotonic All resistors are equal V_{in}* does not supply current Faster- V_{in}* directly connected	Insensitive to CM effects Positive input grounded No high impedance nodes, fast
Disadvantages	Sensitive to CM effects High impedances nodes-only a disadvantage if V_{REF} changes.	More resistor area Can be nonmonotonic Resistor spread of 2^N V_{in}* must supply current More noise because more resistors

Problem 10.8-05

Part of a 6-bit, flash ADC is shown. The comparators have a dominant pole at 10^3 radians/sec, a dc gain of 10^4 a slew rate of 3V/μs, and a binary output voltage of 1V and 0V. Assume that the conversion time is the time required for the comparator to go from its initial state to halfway to is final state. What is the maximum conversion rate of this ADC if V_{REF} = 5V? Assume the resistor ladder is ideal.

Solution:

The output of the *i*-th comparator can be found by taking the inverse Laplace transform of,

$$V_{out}(s) = \left(\frac{A_o}{(s/10^3) + 1}\right)\cdot\left(\frac{v_{in}^* - V_{Ri}}{s}\right)$$

to get,

$$v_{out}(t) = A_o(1 - e^{-10^3 t})(v_{in}^* - V_{Ri}).$$

The worst case occurs when

$$v_{in}^* - V_{Ri} = 0.5V_{LSB} = \frac{V_{REF}}{2^7} = \frac{5}{128}$$

$$\therefore\ 0.5V = 10^4(1 - e^{-10^3 T})(5/128) \rightarrow \frac{64}{5\cdot 10^4} = 1 - e^{-10^3 T}$$

$$\text{or, } e^{-10^3 T} = 1 - \frac{64}{50{,}000} = 0.99872 \rightarrow T = 10^{-3}\ln(1.00128) = 2.806\mu s$$

$$\therefore\ \boxed{\text{Maximum conversion rate} = \frac{1}{2.806\mu s} = 0.356\text{x}10^6 \text{ samples/second}}$$

Check the influence of the slew rate on this answer.

$$SR = 3V/\mu s \rightarrow \frac{\Delta V}{\Delta T} = 3V/\mu s \rightarrow \Delta V = 3V/\mu s(2.806\mu s) = 8.42V > 1V$$

Therefore, slew rate does not influence the maximum conversion rate.

Problem 10.8-06

A flash ADC uses op amps as comparators. The power supply to the op amps is +5V and ground. Assume that the output swing of the op amp is from ground to +5V. The range of the analog input signal is from 1V to 4V (V_{REF} = 3V). The op amps are ideal except that the output voltage is given as

$$v_o = 1000\,(v_{id} + V_{OS}) + A_{cm}\,v_{cm}$$

where v_{id} is the differential input voltage to the op amp, A_{cm} is the common mode gain of the op amp, v_{cm} is the common mode input voltage to the op amp, and V_{OS} is the dc input offset voltage of the op amp. (a.) If A_{cm} = 1V/V and V_{OS} = 0V, what is the maximum number of bits that can be converted by the flash ADC assuming everything else is ideal. Use a worst case approach. (b.) If A_{cm} = 0 and V_{OS} = 40mV, what is the maximum number of bits that can be converted by the flash ADC assuming everything else is ideal. Use a worst case approach.

Solution

(a.) $\Delta v_o = 5\text{V} = 1000\Delta v_{id} \pm 1 v_{cm}$

Choose v_{cm} = 4V as the worst case.

$$\therefore \qquad \Delta v_{id} = \frac{5+4}{1000} = \frac{9}{1000} \le \frac{V_{REF}}{2^{N+1}} = \frac{3}{2^{N+1}}$$

$$2^{N+1} \le \frac{1000 \cdot 3}{9} \qquad \rightarrow \qquad 2^N \le \frac{500 \cdot 3}{9} = 167 \qquad \rightarrow \qquad \underline{\underline{N = 7}}$$

(b.) $\Delta v_o = 5\text{V} = 1000\Delta v_{id} \pm 1000 \cdot 40\text{mV}$

$$\Delta v_{id} = \frac{5-(\pm 1000 \cdot 40\text{mV})}{1000} = 5\text{mV} - (\pm 40\text{mV}) = 45\text{mV (worst case)}$$

$$\therefore \qquad 45\text{mV} \le \frac{3}{2^{N+1}} \qquad \rightarrow \qquad 2^N \le \frac{3}{45\text{mV}} \qquad \rightarrow \qquad 2^N \le \frac{3000}{2 \cdot 45} = 33.33$$

$$\therefore \qquad \underline{\underline{N = 5}}$$

Problem 10.8-07

For the interpolating ADC of Fig. 10.8-3, find the accuracy required for the resistors connected between V_{REF} and ground using a worst case approach. Repeat this analysis for the eight series interpolating resistors using a worst case approach.

Solution

All of the resistors must have the accuracy of ±0.5*LSB*. This accuracy is found as

$$INL = 2^{N-1}\frac{\Delta R}{R} < 0.5$$

If N = 3, then

$$2^2 \frac{\Delta R}{R} < 0.5 \qquad \rightarrow \qquad \frac{\Delta R}{R} < \frac{1}{8} = \underline{\underline{12.5\%}}$$

Problem 10.8-08

Assume that the input capacitance to the 8 comparators of Fig. 10.8-6 are equal. Calculate the relative delays from the output of amplifiers A_1 and A_2 to each of the 8 comparator inputs.

Solution

Solve by finding the equivalent resistance seen from each comparator, $R_{eq.}(i)$ This resistance times the input capacitance, C, to each comparator will be proportional to the delay.

$R_{eq.}(1) = 0.25R + R||3R = 0.25R + 0.75R = R$

$R_{eq.}(2) = 2R||2R = R$

$R_{eq.}(3) = 0.25R + R||3R = 0.25R + 0.75R = R$

$R_{eq.}(4) = R$

Similarly,

$R_{eq.}(5) = R$

$R_{eq.}(6) = R$

$R_{eq.}(7) = R$

$R_{eq.}(8) = R$

Therefore, $\tau = R_{eq.}(i)C$ are all equal and all delays are equal.

Problem 10.8-09

What number of comparators are needed for a folding and interpolating ADC that has the number of coarse bits as $n1 = 3$ and the number of fine bits as $n2 = 4$ and uses an interpolation of 4 on the fine bits? How many comparators would be needed for an equivalent 7-bit flash ADC?

Solution

$n1 = 3 \Rightarrow \quad 2^3\text{-}1 = 7$

$n2 = 4 \Rightarrow \quad 2^4\text{-}1 = 15$

Therefore, 21 comparators are needed compared with $2^7\text{-}1 = 127$ for a 7-bit flash.

Problem 10.8-10

Give a schematic for a folder having a single-ended output that varies between 1V and 3V, starts at 1V, ends at 1V and passes through 2V six times.

Solution

See the circuit schematic below.

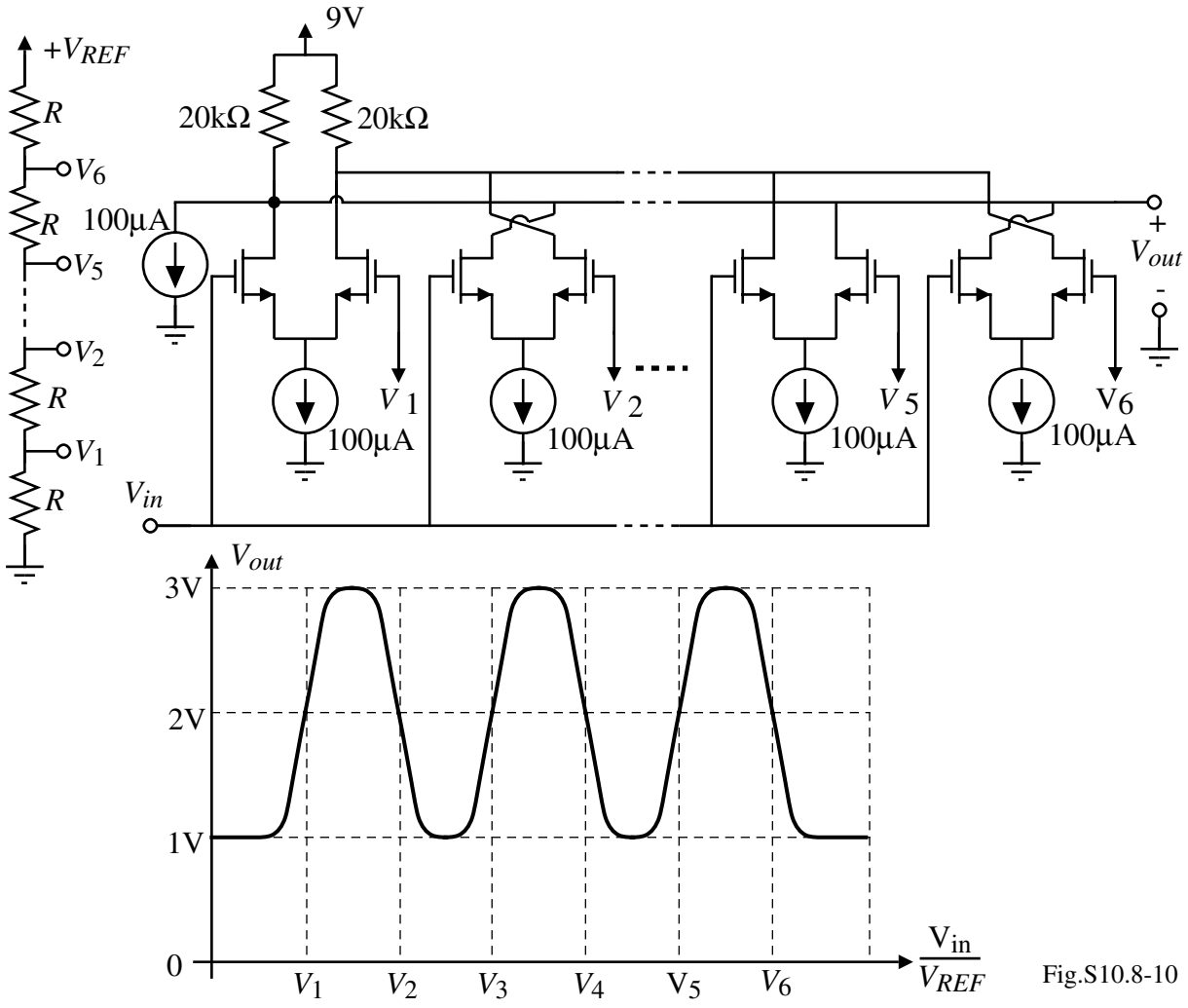
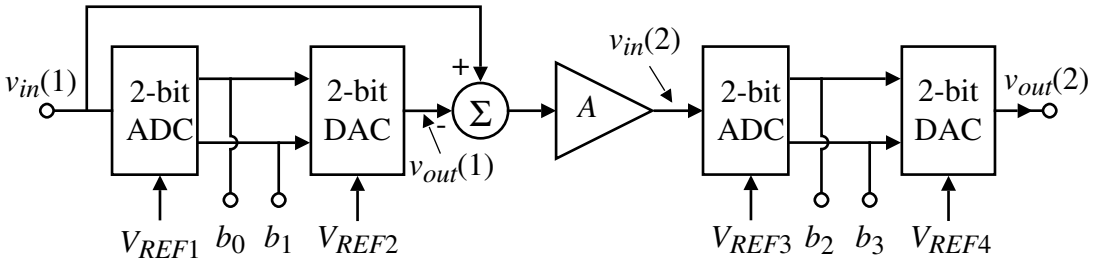


Fig.S10.8-10

Problem 10.8-11

A pipeline, ADC is shown in Fig. P10.8-11. Plot the output-input characteristic of this ADC if $V_{REF1} = 0.75V_{REF}$, $V_{REF2} = V_{REF}$, $V_{REF3} = 0.75V_{REF}$, $V_{REF4} = 1.25V_{REF}$, and $A = 4$. Express the *INL* and the *DNL* in terms of a *+LSB* and a *-LSB* value and determine whether the converter is monotonic or not. (F93E2P2)



Solution

Observations:

∴ First stage changes at $v_{in}(1) = (3/16)V_{REF}$, $(6/16)V_{REF}$, $(9/16)V_{REF}$ and $(12/16)V_{REF}$.

∴ $v_{out}(1) = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF}$

3.) Second stage changes at $v_{in}(2) = (3/16)V_{REF}$, $(6/16)V_{REF}$, $(9/16)V_{REF}$ and $(12/16)V_{REF}$.

4.) $v_{in}(2) = 4[v_{in}(1) - v_{out}(1)]$ or $v_{in}(1) = (1/4)\, v_{in}(2) + v_{out}(1)$

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
0	0	0	0	0	0	0	Starting point
(1/4)x(3/16)=0.75/16	0	0	0	3/16	0	1	
(1/4)x(6/16)=1.50/16	0	0	0	6/16	1	0	
(1/4)x(9/16)=2.25/16	0	0	0	9/16	1	1	
3/16	0	1	4/16	-4/16	0	0	Stage 1 switches
(1/4)x(3/16)+(4/16)=4.75/16	0	1	4/16	3/16	0	1	
(1/4)x(6/16)+(4/16)=5.50/16	0	1	4/16	6/16	1	0	
6/16	1	0	8/16	-8/16	0	0	Stage 1 switches
(1/4)x(3/16)+(8/16)=8.75/16	1	0	8/16	3/16	0	1	
9/16	1	1	12/16	-12/16	0	0	Stage 1 switches
(1/4)x(3/16)+(12/16)=12.75/16	1	1	12/16	3/16	0	1	
(1/4)x(6/16)+(12/16)=13.50/16	1	1	12/16	6/16	1	0	
(1/4)x(9/16)+(12/16)=14.25/16	1	1	12/16	9/16	1	1	

Plot is on the next page.

Problem 10.8-11- Continued

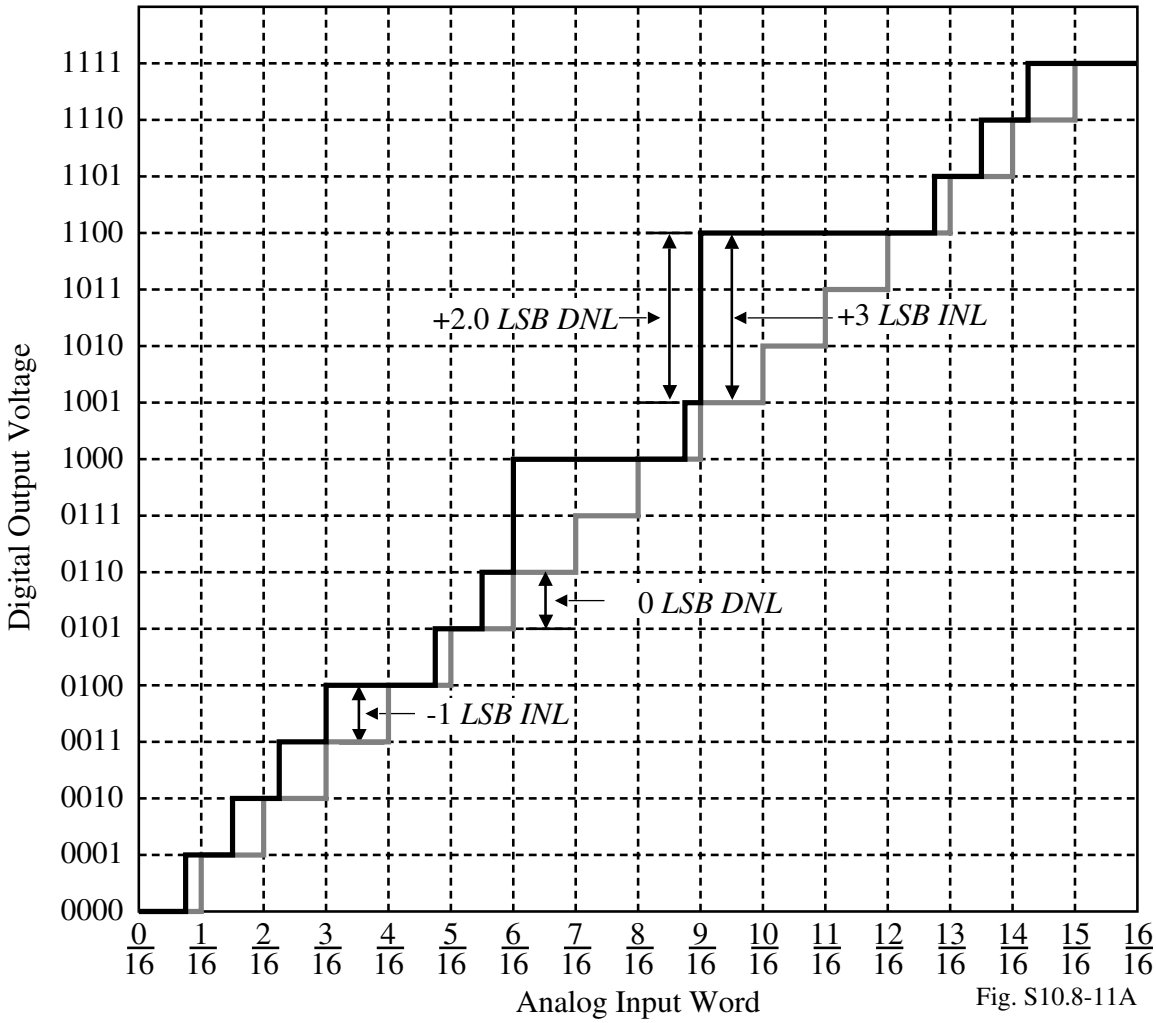
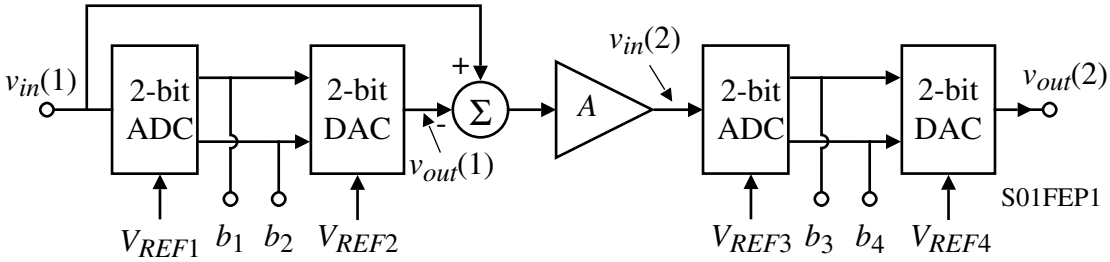


Fig. S10.8-11A

INL: +3*LSB* and –1 *LSB*
DNL: +2*LSB* and 0*LSB*
The ADC is monotonic
The ADC has missing codes which are 0111, 1010, and 1011

Problem 10.8-12

A pipeline, ADC is shown below. Plot the output-input characteristic of this ADC if $V_{REF1} = V_{REF2} = 0.75V_{REF}$ and all else is ideal ($V_{REF3} = V_{REF4} = V_{REF}$ and $A = 4$). Express the *INL* and the *DNL* in terms of a *+LSB* and a *-LSB* value and determine whether the converter is monotonic or not.



Solution

The first stage changes when $v_{in}(1) = \frac{3}{16}V_{REF}$, $\frac{6}{16}V_{REF}$, $\frac{9}{16}V_{REF}$, and $\frac{12}{16}V_{REF}$.

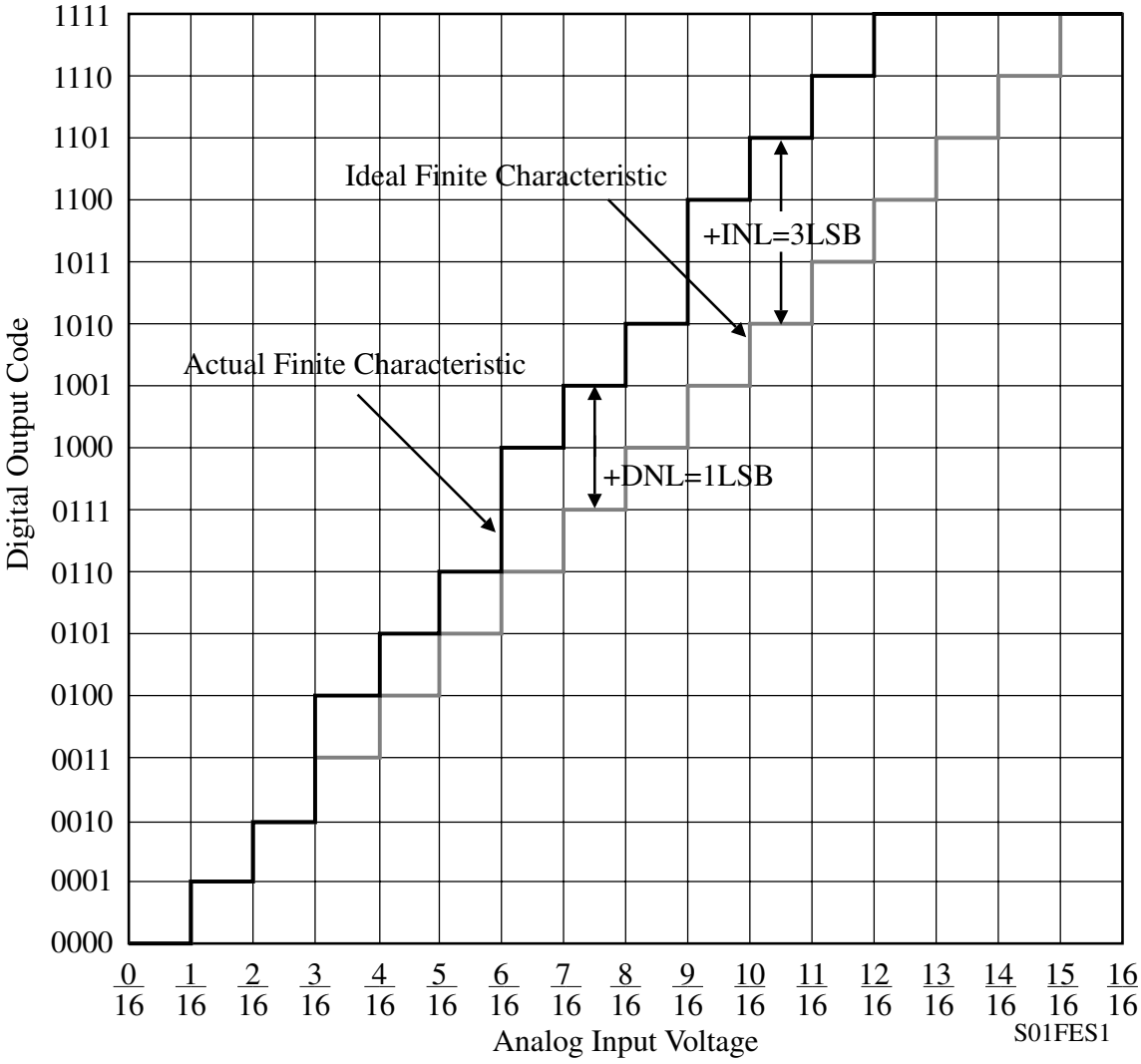
The second stage changes when $v_{in}(2) = \frac{4}{16}V_{REF}$, $\frac{8}{16}V_{REF}$, $\frac{12}{16}V_{REF}$, and $\frac{16}{16}V_{REF}$.

Therefore,

$v_{in}(1)$	b_1	b_2	$v_{out}(1)$	$v_{in}(2) = 4v_{in}(1)–4v_{out}(1)$	b_3	b_4
0	0	0	0	0	0	0
1/16	0	0	0	4/16 = 1/4	0	1
2/16	0	0	0	8/16 = 2/4	1	0
3/16	0	1	3/16	12/16-12/16 = 0	0	0
4/16	0	1	3/16	16/16-12/16 = 4/16	0	1
5/16	0	1	3/16	20/16-12/16 = 8/16	1	0
6/16	1	0	6/16	24/16-24/16 = 0	0	0
7/16	1	0	6/16	28/16-24/16 = 4/16	0	1
8/16	1	0	6/16	32/16-24/16= 8/16	1	0
9/16	1	1	9/16	36/16-36/16	0	0
10/16	1	1	9/16	40/16-36/16 = 4/16	0	1
11/16	1	1	9/16	44/16-36/16 = 8/16	1	0
12/16	1	1	9/16	48/16-36/16 12/16	1	1
13/16	1	1	9/16	52/16-36/16 = 16/16	1	1
14/16	1	1	9/16	56/16-36/16 = 20/16	1	1
15/16	1	1	9/16	60/16-36/16 = 24/16	1	1

Problem 10.8-12 - Continued

ADC Characteristic Plot:



From the above plot we see that:

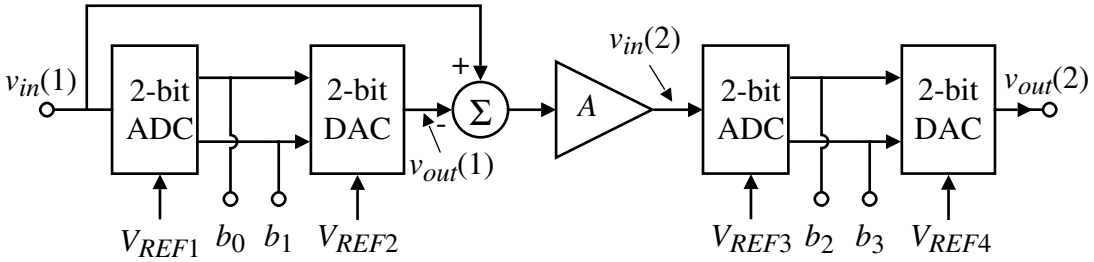
$+INL = 3\text{LSB}$, $-INL = 0\text{LSB}$, $+DNL = 1\text{LSB}$ and $-DNL = 0\text{LSB}$

(Note that we cannot say that the ADC has –1LSB for *–DNL* when the ADC saturates.)

The ADC is monotonic.

Problem 10.8-13

Repeat Problem 11 if (a.) $A = 2$ and (b.) $A = 6$ and all other values of the ADC are ideal.



Solution

(a.) $A = 2$. Observations:

∴ First stage changes at $v_{in}(1) = (4/16)V_{REF}$, $(8/16)V_{REF}$, and $(12/16)V_{REF}$.

∴ $v_{out}(1) = \left(\frac{b_0}{2} + \frac{b_1}{4}\right)V_{REF}$

3.) 2nd stage changes at $v_{in}(2) = (4/16)V_{REF}$, $(8/16)V_{REF}$, and $(12/16)V_{REF}$.

4.) $v_{in}(2) = 2[v_{in}(1) - v_{out}(1)]$ or $v_{in}(1) = (1/2)\, v_{in}(2) + v_{out}(1)$

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
0	0	0	0	0	0	0	Starting point
(1/2)x(4/16)=2/16	0	0	0	4/16	0	1	
(1/2)x(8/16)=4/16	0	1	4/16	0	0	0	Stage 1 switches
(1/2)x(4/16)+(4/16)=6/16	0	1	4/16	4/16	0	1	
(1/2)x(8/16)+(4/16)=8/16	1	0	8/16	0	0	0	Stage 1 switches
(1/2)x(4/16)+(8/16)=10/16	1	0	8/16	4/16	0	1	
(1/2)x(8/16)+(8/16)=12/16	1	1	12/16	0	0	0	Stage 1 switches
(1/2)x(4/16)+(12/16)=14/16	1	1	12/16	4/16	0	1	

With a gain of 2, the second stage sees $v_{in}(2) = 2[v_{in}(1) - v_{out}(1)]$. $v_{in}(2)$ will never exceed $0.25V_{REF}$ before the first stage output brings $v_{in}(2)$ back to zero. As a consequence, b_2 is stuck at zero. The plot is on the next page. It can seen from the plot that INL =+0LSB and –2LSB , DNL = +2LSB and –0LSB. The ADC is monotonic.

(b.) $A = 6$. $v_{in}(2) = 6[v_{in}(1) - v_{out}(1)]$ or $v_{in}(1) = (1/6)\, v_{in}(2) + v_{out}(1)$

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
0	0	0	0	0	0	0	Starting point
(1/6)x(4/16)=0.667/16	0	0	0	4/16	0	1	
(1/6)x(8/16) = 1.333/16	0	0	0	8/16	1	0	
(1/6)x(12/16)=2/16	0	0	0	12/16	1	1	
4/16	0	1	4/16	0	0	0	Stage 1 switches
(1/6)x(4/16)+(4/16)=4.667/16	0	1	4/16	4/16	0	1	

Problem 10.8-13 – Continued

Value of $v_{in}(1)$ where a change occurs	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3	Comments
(1/6)x(8/16)+(4/16)=5.333/16	0	1	4/16	8/16	1	0	
(1/6)x(12/16)+(4/16)=6/16	0	1	4/16	12/16	1	1	
8/16	1	0	8/16	0	0	0	Stage 1 switches
(1/6)x(4/16)+(8/16)=8.667/16	1	0	8/16	4/16	0	1	
(1/6)x(8/16)+(8/16)=9.333/16	1	0	8/16	8/16	1	0	
(1/6)x(12/16)+(8/16)=10/16	1	0	8/16	12/16	1	1	
12/16	1	1	12/16	0	0	0	Stage 1 switches
(1/6)x(4/16)+(12/16)=12.667/16	1	1	12/16	4/16	0	1	
(1/6)x(8/16)+(12/16)=13.333/16	1	1	12/16	8/16	1	0	
(1/6)x(12/16)+(12/16)=14/16	1	1	12/16	12/16	1	1	

It can seen from the plot below that *INL* =+1*LSB* and –0*LSB*, *DNL* = ±0*LSB*. The ADC is monotonic.

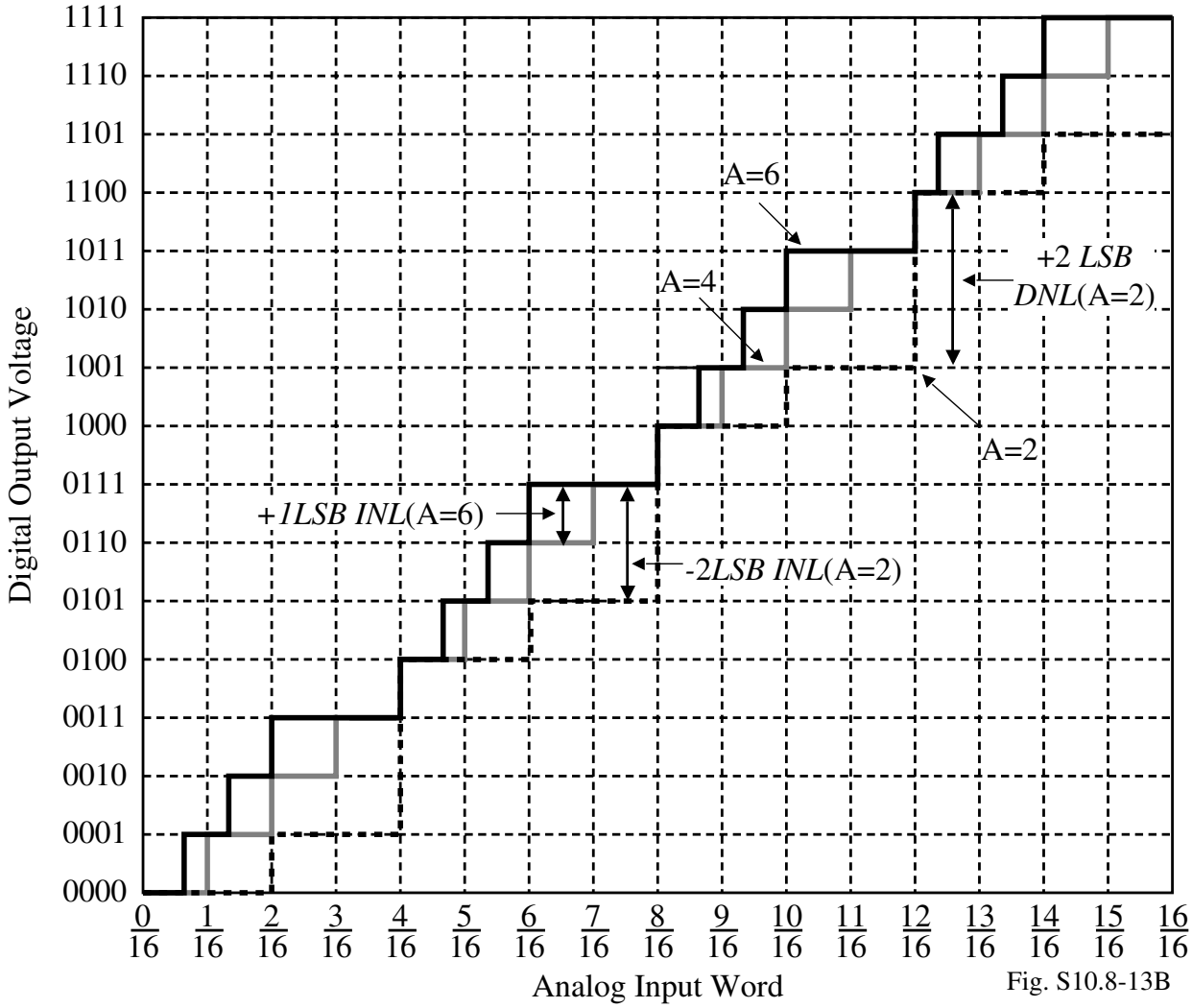
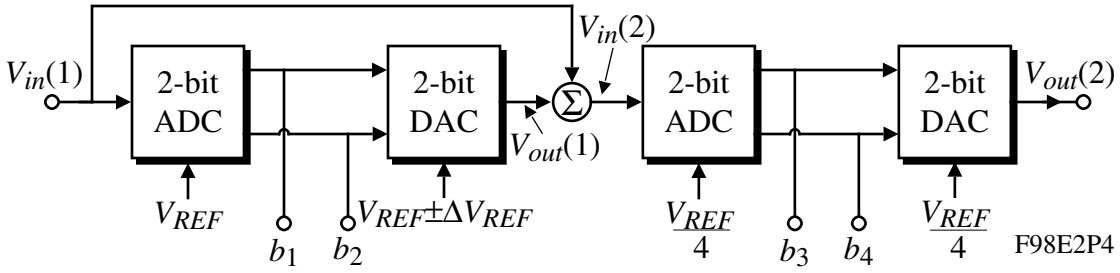


Fig. S10.8-13B

Problem 10.8-14

For the pipeline ADC shown, the reference voltage to the DAC of the first stage is $V_{REF} \pm \Delta V_{REF}$. If all else is ideal, what is the smallest value of ΔV_{REF} that will keep the *INLA* to within (a.) $\pm 0.5LSB$ and (b.) $\pm 1LSB$?



Solution

$$V_{out}(1) = \text{Ideal} \pm \text{Error} = \left(\frac{b_1}{2} + \frac{b_2}{4}\right) V_{REF} \pm \left(\frac{b_1}{2} + \frac{b_2}{4}\right) \Delta V_{REF}$$

$$V_{out}(2) = V_{in}(1) - V_{out}(1) = V_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right) V_{REF} \pm \left(\frac{b_1}{2} + \frac{b_2}{4}\right) \Delta V_{REF}$$

The second stage switches at $V_{REF}/16$, $2V_{REF}/16$, $3V_{REF}/16$, and $4V_{REF}/16$.

Therefore the *LSB* is $V_{REF}/16$.

(a.) $INLA = \pm 0.5LSB$

$$\left(\frac{b_1}{2} + \frac{b_2}{4}\right) \Delta V_{REF} \le \frac{\pm V_{REF}}{32}$$

When b_1 and b_2 are both 1 corresponds to the worst case.

$$\therefore \quad \boxed{\Delta V_{REF} \le \frac{4}{3} \frac{\pm V_{REF}}{32} = \frac{\pm V_{REF}}{24}}$$

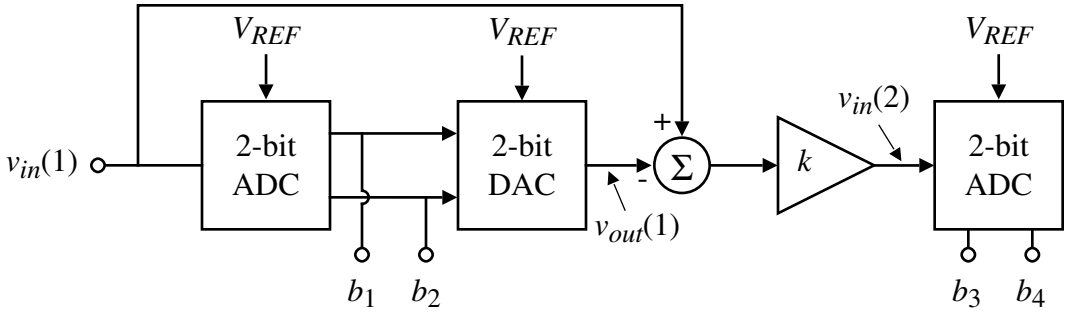
(b.) $INLA = \pm 0.5LSB$

$$\left(\frac{b_1}{2} + \frac{b_2}{4}\right) \Delta V_{REF} \le \frac{\pm V_{REF}}{16}$$

$$\therefore \quad \boxed{\Delta V_{REF} \le \frac{4}{3} \frac{\pm V_{REF}}{16} = \frac{\pm V_{REF}}{12}}$$

Problem 10.8-15

A 4-bit ADC consisting of two, 2-bit stages (pipes) is shown. Assume that the 2-bit ADC's and the 2-bit DAC function ideally. Also, assume that $V_{REF} = 1V$. The ideal value of the scaling factor, k, is 4. Find the maximum and minimum value of k that will not cause an error in the 4-bit ADC. Express the tolerance of k in terms of a plus and minus percentage.



Solutions

The input to the second ADC is $v_{in}(2) = k\left[v_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right]$.

If we designate this voltage as $v'_{in}(2)$ when $k = 4$, then the difference between $v_{in}(2)$ and $v'_{in}(2)$ must be less than ±1/8 or the *LSB* bits will be in error.

Therefore:

$$\left|v_{in}(2) - v'_{in}(2)\right| = \left|k\ v_{in}(1) - k\left(\frac{b_1}{2} + \frac{b_2}{4}\right) - 4\ v_{in}(1) + 4\left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right| \le \frac{1}{8}$$

If $k = 4 + \Delta k$, then

$$\left|4\ v_{in}(1) + \Delta k\ v_{in}(1) - 4\left(\frac{b_1}{2} + \frac{b_2}{4}\right) - \Delta k\left(\frac{b_1}{2} + \frac{b_2}{4}\right) - 4\ v_{in}(1) + 4\left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right| \le \frac{1}{8}$$

or

$$\Delta k\left|v_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right| \le \frac{1}{8}\ .$$

The largest value of $\left|v_{in}(1) - \left(\frac{b_1}{2} + \frac{b_2}{4}\right)\right|$ is 1/4 for any value of $v_{in}(1)$ from 0 to V_{REF}. Therefore,

$$\frac{\Delta k}{4} \le \frac{1}{8} \ \Rightarrow\ \Delta k \le 1/2.$$

Therefore the tolerance of k is $\boxed{\frac{\Delta k}{k} = \frac{\pm 1}{2 \cdot 4} = \frac{\pm 1}{8} \Rightarrow \pm 12.5\%}$

Problem 10.8-16

The pipeline, analog-to-digital converter shown in Fig. P10.8-16 uses two identical, ideal, two-bit stages to achieve a 4-bit analog-to-digital converter. Assume that the bits, b_2 and b_3, have been mistakenly interchanged inside the second-stage ADC. Plot the output-input characteristics of the converter, express the INL and DNL in terms of a +LSB and a -LSB, and determine whether the converter is monotonic or not.

Solution

$v_{in}(1)$	b_0	b_1	$v_{out}(1)$	$v_{in}(2)$	b_2	b_3
0	0	0	0	0	0	0
1/16	0	0	0	1/16	1	0
2/16	0	0	0	2/16	0	1
3/16	0	0	0	3/16	1	1
4/16	0	1	4/16	0	0	0
5/16	0	1	4/16	1/16	1	0
6/16	0	1	4/16	2/16	0	1
7/16	0	1	4/16	3/16	1	1
8/16	1	0	8/16	0	0	0
9/16	1	0	8/16	1/16	1	0
10/16	1	0	8/16	2/16	0	1
11/16	1	0	8/16	3/16	1	1
12/16	1	1	12/16	0	0	0
12/16	1	1	12/16	1/16	1	0
13/16	1	1	12/16	2/16	0	1
14/16	1	1	12/16	3/16	1	1

The plot on the next page shows that the $INL = \pm 1LSB$ and $DNL = +1LSB$ and $-2LSB$. The ADC is not monotonic.

Problem 10.8-16 – Continued

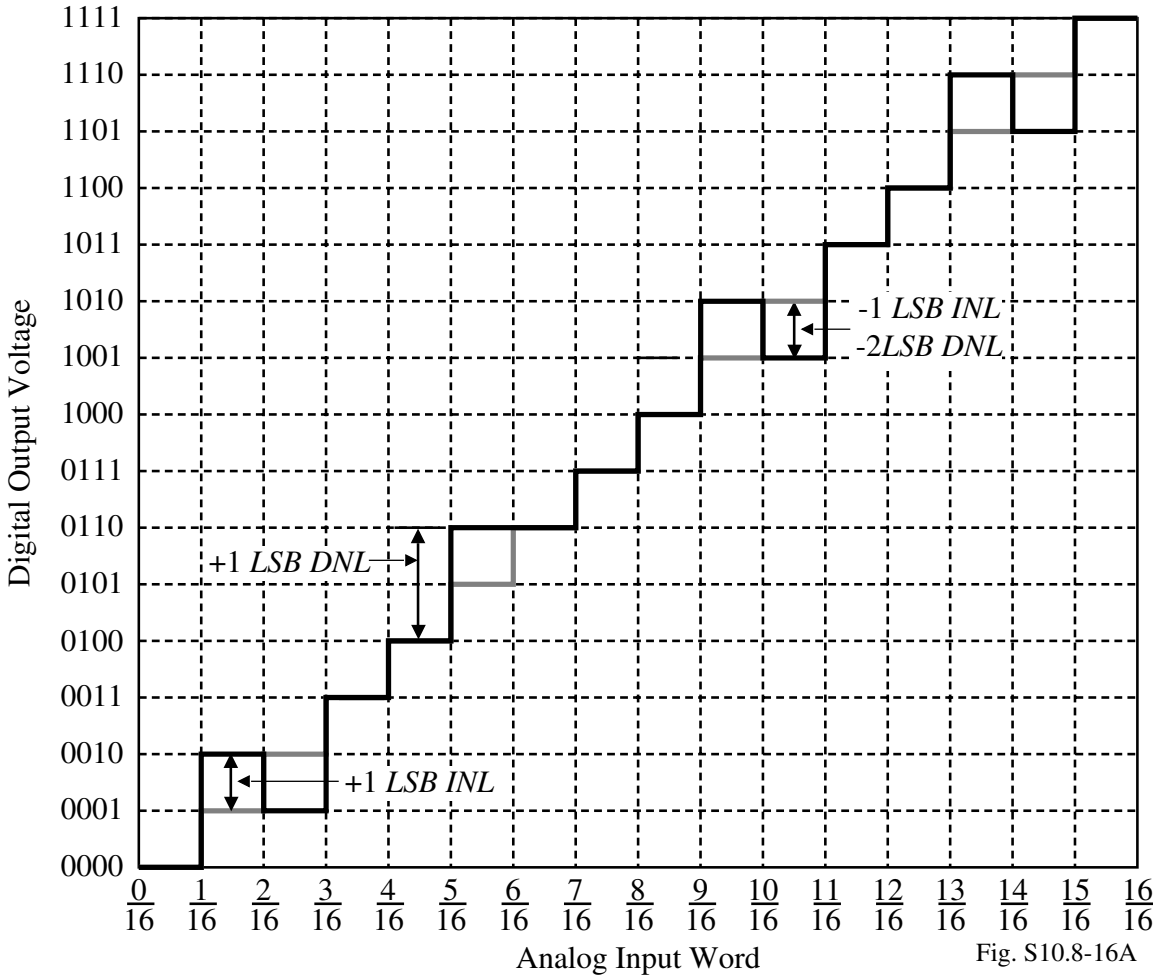


Fig. S10.8-16A

Problem 10.9-01

A first-order, delta-sigma modulator is shown in Fig. P10.9-1. Find the magnitude of the output spectral noise with $V_{in}(z) = 0$ and determine the bandwidth of a 10-bit analog-to-digital converter if the sampling frequency, f_s, is 10 MHz and k = 1. Repeat for k = 0.5.

Solution

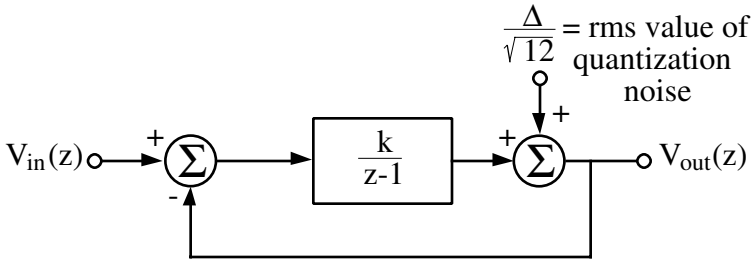


Figure P10.9-1

From the block diagram, we can write,

$$V_{out}(z) = \frac{\Delta}{\sqrt{12}} + \frac{k}{z\text{-}1}\left[V_{in}(z) - V_{out}(z)\right]$$

Solving for $V_{out}(z)$ gives,

$$V_{out}(z) = \left(\frac{z\text{-}1}{z\text{-}1+k}\right)\left[\frac{\Delta}{\sqrt{12}} + \frac{kV_{in}(z)}{z\text{-}1}\right] = \left(\frac{z\text{-}1}{z\text{-}1+k}\right)\frac{\Delta}{\sqrt{12}} \quad \text{if } V_{in}(z) = 0$$

$$\therefore \qquad H(z) = \left(\frac{z\text{-}1}{z\text{-}1+k}\right) \qquad \rightarrow \qquad H(e^{j\omega T}) = \frac{e^{j\omega T} - 1}{e^{j\omega T} - 1 + k} = \frac{e^{j\omega T/2} - e^{-j\omega T/2}}{e^{j\omega T/2} - e^{-j\omega T/2} + ke^{-j\omega T/2}}$$

$$H(e^{j\omega T}) = \frac{2j\sin(\omega T/2)}{2j\sin(\omega T/2) + k[\cos(\omega T/2) - j\cos(\omega T/2)]} = \frac{2\tan(\omega T/2)}{(2-k)\tan(\omega T/2) - jk}$$

Find the bandwidth by setting $|H(e^{j\omega T})|^2 = 0.5$.

$$|H(e^{j\omega T})|^2 = \frac{4\tan^2(\omega T/2)}{(2-k)^2\tan^2(\omega T/2) + k^2} = 0.5 \rightarrow \; 8\tan^2(\omega T/2) = (2-k)^2\tan^2(\omega T/2) + k^2$$

$$\tan^2(\omega T/2)[8 - (2-k)^2] = k^2 \quad \rightarrow \qquad \omega T/2 = \tan^{-1}\left[\sqrt{\frac{k^2}{8 - (2-k)^2}}\right]$$

$$\omega = \frac{2}{T}\tan^{-1}\left[\frac{k}{\sqrt{8 - (2-k)^2}}\right] = 2f_s\tan^{-1}\left[\frac{k}{\sqrt{8 - (2-k)^2}}\right]$$

For $k = 1$,

$$\omega_{-3dB} = 2f_s\tan^{-1}\left[\frac{1}{\sqrt{4}}\right] = \underline{\underline{0.927\text{x}10^7 \text{ rads/sec} \rightarrow 1.476 \text{ MHz}}}$$

For $k = 0.5$,

$$\omega_{-3dB} = 2f_s\tan^{-1}\left[\frac{0.5}{\sqrt{8 - \frac{9}{4}}}\right] = \underline{\underline{0.411\text{x}10^7 \text{ rads/sec} \rightarrow 0.654 \text{ MHz}}}$$

Note that the results are independent of the number of bits because *H* is the noise transfer function.

Problem 10.9-02

The specification for an oversampled analog-to-digital converter is 16-bits with a bandwidth of 100kHz and a sampling frequency of 10MHz. (a.) What is the minimum number of loops in a Sodini modulator using a 1-bit quantizer ($\Delta=V_{REF}/2$) that will meet this specification? (b.) If the Sodini modulator has two loops, what is the minimum number of bits for the quantizer to meet the specification?

Solution

The general formula for the L-th order Sodini loop is,

$$n_o = \frac{\Delta}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{2f_B}{f_s} \right)^{L+0.5}$$

(a.) Δ(quantizer) = $0.5V_{REF}$ and an $LSB = \dfrac{V_{REF}}{2^{16}}$

$$\therefore \quad n_o = \leq LSB \quad \Rightarrow \quad \frac{V_{REF}}{2\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{200}{10{,}000} \right)^{L+0.5} \leq \frac{V_{REF}}{2^{16}}$$

or

$$\frac{2^{15}}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{1}{50} \right)^{L+0.5} \leq 1 \quad \Rightarrow \quad \underline{\underline{L \geq 3}}$$

(b.) Δ(quantizer) = $\dfrac{V_{REF}}{2^b}$, where b = no. of bits

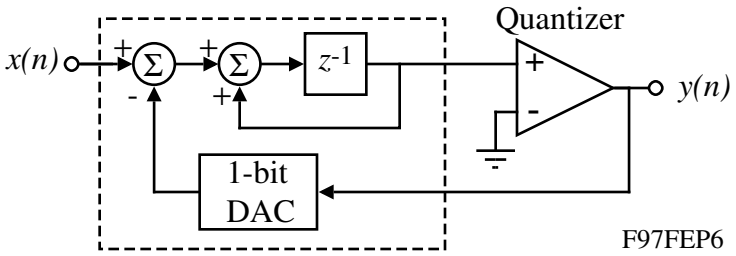
$$\therefore \quad n_o = \frac{V_{REF}}{2^b} \frac{\pi^2}{\sqrt{12}\sqrt{5}} \left(\frac{1}{50} \right)^{2.5} \leq \frac{V_{REF}}{2^{16}}$$

$$2^b \geq \frac{2^{16}\pi^2}{\sqrt{12}\sqrt{5}} \left(\frac{1}{50} \right)^{2.5} = 4.7237$$

$$\therefore \quad \underline{\underline{b = 3}}$$

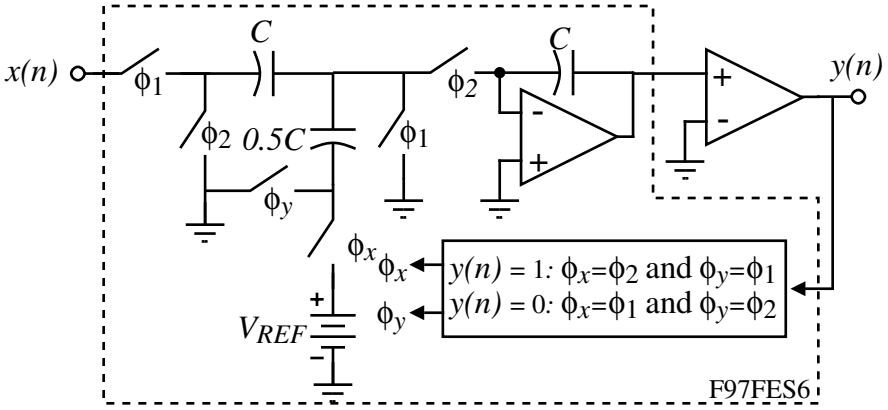
Problem 10.9-03

Draw a single-ended switched capacitor realization of everything within the dashed box of the delta-sigma modulator. Assume that the output of the 1-bit DAC is $\pm 0.5V_{REF}$. Be sure to show the phases of the switches (ϕ_1 and ϕ_2).



Solution

Note that the inner loop is equal to $\frac{z^{-1}}{1-z^{-1}}$ which is a switched capacitor noninverting integrator. Therefore a possible realization of the dashed box is shown below.



Problem 10.9-04

The modulation noise spectral density of a second-order, 1-bit ΣΔ modulator is given as

$$|N(f)| = \frac{4\Delta}{\sqrt{12}}\sqrt{\frac{2}{f_s}}\ \sin^2\left(\frac{\omega\tau}{4}\right)$$

where Δ is the signal level out of the 1-bit quantizer and $f_s = (1/\tau)$ = the sampling frequency and is 10MHz. Find the signal bandwidth, f_B, in Hz if the modulator is to be used in an 18 bit oversampled ADC. Be sure to state any assumption you use in working this problem.

Solution

The rms noise in the band 0 to f_B can be found as,

$$n_o^2 = \int_0^{f_B} |N(f)|^2 df = \frac{16\Delta^2}{12}\frac{2}{f_s}\int_0^{f_B} \sin^4\left(\frac{\omega}{4f_s}\right) df$$

Assume that $\frac{\omega}{4f_s} = \frac{2\pi f}{4f_s} = \frac{\pi f}{2f_s} << 1$ so that $\sin^4\left(\frac{\omega}{4f_s}\right) \approx \frac{\omega}{4f_s}$

$$\therefore \quad n_o^2 = \frac{8}{3}\frac{\Delta^2}{f_s}\int_0^{f_B}\left(\frac{2\pi f}{4f_s}\right)^4 df = = \frac{8}{3}\frac{\Delta^2}{f_s}\left(\frac{\pi^4}{16{f_s}^4}\right)\int_0^{f_B} f^4\ df$$

$$= \frac{8}{3}\frac{\Delta^2\pi^4}{16}\frac{1}{5}\left(\frac{f_B}{f_s}\right)^5 = \frac{8}{15}\frac{\Delta^2\pi^4}{16}\left(\frac{f_B}{f_s}\right)^5$$

$$n_o = \sqrt{\frac{8}{15}}\frac{\Delta\pi^2}{4}\left(\frac{f_B}{f_s}\right)^{5/2}$$

Assume that $\Delta \approx V_{REF}$. For an 18-bit converter, we get

$$n_o \le \frac{V_{REF}}{2^{18}} = \frac{\Delta}{2^{18}} \quad \rightarrow \quad \sqrt{\frac{8}{15}}\frac{\Delta\pi^2}{4}\left(\frac{f_B}{f_s}\right)^{5/2} \le \frac{\Delta}{2^{18}}$$

$$\left(\frac{f_B}{f_s}\right)^{5/2} \le \sqrt{\frac{15}{8}}\frac{4}{\Delta\pi^2}\frac{1}{2^{18}} = \frac{0.555}{2^{18}} = 2.117\text{x}10^{-6}$$

$$\frac{f_B}{f_s} \le 0.005373 \quad \rightarrow \quad \underline{\underline{f_B = 53.74\ \text{kHz}}}$$

Problem 10.9-05

The noise power in the signal band of zero to f_B of a L-th order, oversampling ADC is given as

$$n_o = \frac{\Delta}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{2f_B}{f_s} \right)^{L+0.5}$$

where f_s is the sampling frequency.

$$\Delta = \frac{V_{REF}}{2^b}$$

and b is the number of bits of the quantizer. Find the minimum oversampling ratio, OSR (=f_s/f_B), for the following cases:

(a.) A 1-bit quantizer, third-order loop, 16 bit oversampled ADC.

(b.) A 2-bit quantizer, third-order loop, 16 bit oversampled ADC.

(c.) A 3-bit quantizer, second-order loop, 16 bit oversampled ADC.

Solution

(a.) $$n_o = \frac{V_{REF}}{2\sqrt{12}} \frac{\pi^3}{\sqrt{7}} \left(\frac{2f_B}{f_s} \right)^{3.5} \le \frac{V_{REF}}{2^{16}} \rightarrow \left(\frac{f_B}{f_s} \right)^{3.5} \le \frac{\sqrt{42}}{\pi^3 2^{18}} = 7.9732\text{x}10^{-7} \rightarrow \frac{f_B}{f_s} \le 0.0181$$

$$\therefore \quad \boxed{\frac{f_s}{f_B} = \text{OSR} \ge 55.26}$$

(b.) $$n_o = \frac{V_{REF}}{2^2\sqrt{12}} \frac{\pi^3}{\sqrt{7}} \left(\frac{2f_B}{f_s} \right)^{3.5} \le \frac{V_{REF}}{2^{16}} \rightarrow \left(\frac{f_B}{f_s} \right)^{3.5} \le \frac{\sqrt{42}}{\pi^3 2^{17}} = 1.5946\text{x}10^{-6} \rightarrow \frac{f_B}{f_s} \le 0.0221$$

$$\therefore \quad \boxed{\frac{f_s}{f_B} = \text{OSR} \ge 45.33}$$

(c.) $$n_o = \frac{V_{REF}}{2^3\sqrt{12}} \frac{\pi^3}{\sqrt{5}} \left(\frac{2f_B}{f_s} \right)^{2.5} \le \frac{V_{REF}}{2^{16}} \rightarrow \left(\frac{f_B}{f_s} \right)^{2.5} \le \frac{\sqrt{30}}{\pi^2 2^{15}} = 1.6936\text{x}10^{-5} \rightarrow \frac{f_B}{f_s} \le 0.0123$$

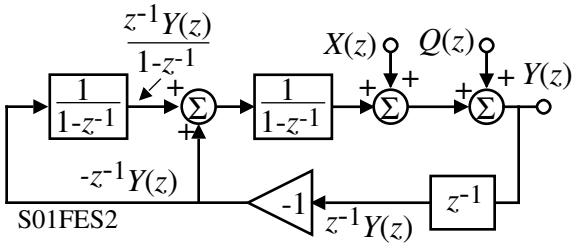
$$\therefore \quad \boxed{\frac{f_s}{f_B} = \text{OSR} \ge 81.00}$$

Problem 10.9-06

A second-order oversampled modulator is shown below. (a.) Find the noise transfer function, $Y(z)/Q(z)$. (b.) Assume that the quantizer noise spectral density of a 1-bit Σ-Δ modulator (not necessarily the one shown below) is

$$|N(f)| = \frac{2V_{REF}}{\sqrt{12}}\sqrt{\frac{2}{f_s}}\ \sin^2\left(\frac{\omega}{2f_s}\right)$$

where f_s = 10MHz and is the sampling frequency. Find the maximum signal bandwidth, f_B, in Hz if the Σ-Δ modulator is used in a 16-bit oversampled analog-to-digital converter.



Solution

(a.) $$Y(z) = Q(z) + X(z) + z^{-1}Y(z) + \left(\frac{1}{1-z^{-1}}\right)\left[-z^{-1}Y(z) - \frac{z^{-1}Y(z)}{1-z^{-1}}\right]$$

$$Y(z) = Q(z) + X(z) + z^{-1}Y(z) - \frac{z^{-1}}{1-z^{-1}}Y(z) - \frac{z^{-1}}{(1-z^{-1})^2}Y(z)$$

$$Y(z)\left[1-z^{-1}+\frac{z^{-1}}{1-z^{-1}}+\frac{z^{-1}}{(1-z^{-1})^2}\right] = Y(z)\left[\frac{1-2z^{-1}+z^{-2}+z^{-1}-z^{-2}+z^{-1}}{(1-z^{-1})^2}\right] = Q(z) + X(z)$$

$$\therefore \quad Y(z) = (1-z^{-1})^2[Q(z) + X(z)] \quad \Rightarrow \quad \boxed{\frac{Y(z)}{Q(z)} = (1-z^{-1})^2}$$

(b.) $$n_o^2 = \int_0^{f_B}|N(f)|^2 df = \frac{4V_{REF}^2}{12}\frac{2}{f_s}\int_0^{f_B} sin^4\left(\frac{\pi f}{f_s}\right)df \approx \frac{2V_{REF}^2}{3f_s}\int_0^{f_B}\left(\frac{\pi f}{f_s}\right)^4 df$$

$$n_o^2 = \frac{2\pi^4 V_{REF}^2}{3f_s^5}\int_0^{f_B} f^4 df = \frac{2\pi^4 V_{REF}^2}{15f_s^5}f_B^5 = \frac{2\pi^4 V_{REF}^2}{15}\left(\frac{f_B}{f_s}\right)^5$$

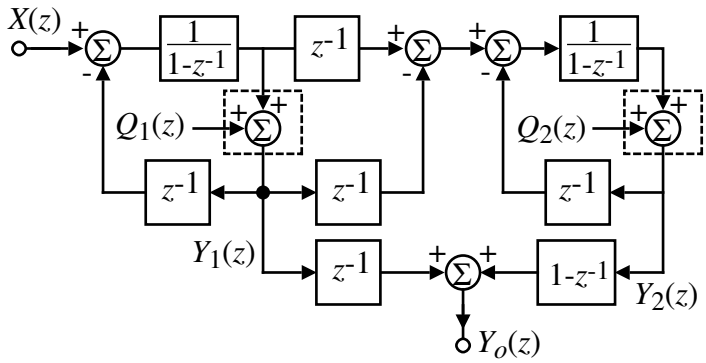
$$n_o = \sqrt{\frac{2}{15}}V_{REF}\pi^2\left(\frac{f_B}{f_s}\right)^5 \le \frac{V_{REF}}{2^{16}}$$

$$\therefore \quad \left(\frac{f_B}{f_s}\right)^{5/2} \le \sqrt{\frac{15}{2}}\frac{1}{\pi^2}\frac{1}{2^{16}} = \frac{0.2775}{2^{16}} = 4.234\text{x}10^{-6}$$

$$\left(\frac{f_B}{f_s}\right) \le (4.234\text{x}10^{-6})^{2/5} = 0.0072 \quad \Rightarrow \quad f_B \le \underline{\underline{70.909\text{kHz}}}$$

Problem 10.9-07

Find an expression for the output, $Y_o(z)$, in terms of the input, $X(z)$, and the quantization noise sources, $Q_1(z)$ and $Q_2(z)$, for the multi-stage Σ-Δ modulator shown in Fig. P10.9-7. What is the order of this modulator?



Solution

First, find $Y_1(z)$ and $Y_2(z)$.

$$Y_1(z) = Q_1(z) + \frac{1}{1-z^{-1}}[X(z) - z^{-1}Y_1(z)] = Q_1(z) + \frac{X(z)}{1-z^{-1}} - \frac{z^{-1}Y_1(z)}{1-z^{-1}}$$

$$Y_1(z)\left[1 + \frac{z^{-1}}{1-z^{-1}}\right] = Q_1(z) + \frac{X(z)}{1-z^{-1}} \quad \Rightarrow \quad Y_1(z) = (1-z^{-1})Q_1(z) + X(z)$$

$$Y_2(z) = Q_1(z) + \frac{1}{1-z^{-1}}\left[-z^{-1}Y_2(z) - z^{-1}Y_1(z) + \frac{z^{-1}}{1-z^{-1}}[X(z) - z^{-1}Y_1(z)]\right]$$

$$Y_2(z)\left[1 + \frac{z^{-1}}{1-z^{-1}}\right] = Q_2(z) + \frac{z^{-1}X(z)}{(1-z^{-1})^2} - \frac{z^{-2}Y_1(z)}{(1-z^{-1})^2} - \frac{z^{-1}Y_1(z)}{1-z^{-1}}$$

$$Y_2(z) = (1-z^{-1})Q_2(z) + \frac{z^{-1}X(z)}{1-z^{-1}} - Y_1(z)\left[z^{-1} + \frac{z^{-2}}{1-z^{-1}}\right]$$

$$Y_2(z) = (1-z^{-1})Q_2(z) + \frac{z^{-1}X(z)}{1-z^{-1}} - \frac{z^{-1}Y_1(z)}{1-z^{-1}}$$

$\therefore$ $Y_o(z) = z^{-1}Y_1(z) + (1-z^{-1})Y_2(z)$

$$= z^{-1}(1-z^{-1})Q_1(z) + z^{-1}X(z) + (1-z^{-1})^2Q_2(z) + z^{-1}X(z) - z^{-1}Y_1(z)$$

$$= z^{-1}(1-z^{-1})Q_1(z) + z^{-1}X(z) + (1-z^{-1})^2Q_2(z) + z^{-1}X(z) - z^{-1}(1-z^{-1})Q_1(z) - z^{-1}X(z)$$

$$\boxed{Y_o(z) = z^{-1}X(z) + (1-z^{-1})^2Q_2(z)}$$

Therefore, the modulator is second-order.

Problem 10.9-08

Two ΔΣ first-order modulators are multiplexed as shown below. $\Delta\Sigma_1$ provides its 1-bit quantizer output during clock phase ϕ_1 and $\Delta\Sigma_2$ provides its 1-bit quantizer output during clock phase ϕ_2 where ϕ_1 and ϕ_2 are nonoverlapping clocks. The noise, n_o, of a general L-loop ΔΣ modulator is

$$n_o = \frac{\Delta}{\sqrt{12}} \frac{\pi^L}{\sqrt{2L+1}} \left(\frac{2f_B}{f_S} \right)^{L+0.5}$$

(a.) Assume that the quantization level for each quantizer is $\Delta = 0.5V_{REF}$ and find the dynamic range in dB that would result if the clock frequency is 100MHz and the bandwidth of the resulting ADC is 1MHz.

(b.) What would the dynamic range be in dB if the quantizers are 2-bit?

Solution:

(a.) If the $\Delta\Sigma_1$ modulator outputs a pulse during ϕ_1 and the $\Delta\Sigma_2$ modulator outputs a pulse during ϕ_2, then two samples occur in 10 ns which is effectively an output pulse rate of $200\text{x}10^6$ pulses/sec which corresponds to a sampling rate of 200MHz. Therefore,

$$n_o = \frac{V_{REF}}{2\sqrt{12}} \frac{\pi}{\sqrt{3}} \left(\frac{2 \cdot 100\text{MHz}}{200\text{MHz}} \right)^{1.5} = 261.8\text{x}10^{-6} V_{REF}$$

$$\therefore \quad \frac{V_{REF}}{n_o} = \frac{10^6}{261.8} = 3819.72 \quad \Rightarrow \quad \boxed{\text{Dynamic Range} = 71.64 \text{ dB } (11.94\text{bits})}$$

(b.) A two-bit quantizer gives $\Delta = V_{REF}/4$.

$$\therefore \quad n_o = \frac{V_{REF}}{4\sqrt{12}} \frac{\pi}{\sqrt{3}} \left(\frac{2 \cdot 100\text{MHz}}{200\text{MHz}} \right)^{1.5} = 130.9\text{x}10^{-6} V_{REF}$$

$$\frac{V_{REF}}{n_o} = \frac{10^6}{130.9} = 7{,}639.4 \quad \Rightarrow \quad \boxed{\text{Dynamic Range} = 77.64 \text{ dB } (12.94\text{bits})}$$

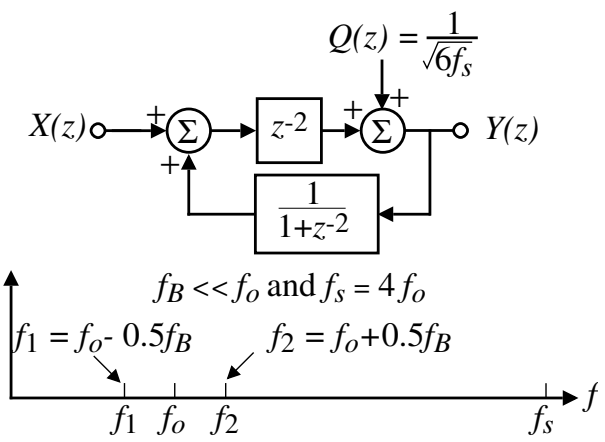
Because n_o is in rms volts, it is consistent to divide V_{REF} by $2\sqrt{2}$ to get

(a.) $$\frac{V_{REF}/2\sqrt{2}}{n_o} = \frac{3819.72}{2\sqrt{2}} = 1350.47 \rightarrow 62.61 \text{ dB}$$

(b.) $$\frac{V_{REF}/2\sqrt{2}}{n_o} = \frac{7639.4}{2\sqrt{2}} = 2700.9 \rightarrow 68.61 \text{ dB}$$

Problem 10.9-09

A first-order, 1-bit, bandpass, ΔΣ modulator is shown in Fig. P10.9-9. Find the modulation noise spectral density, N(f), and integrate the square of the magnitude of N(f) over the bandwidth of interest (f_1 to f_2) and find an expression for the noise power, $n_o(f)$, in the bandwidth of interest in terms of Δ and the oversampling factor M where $M = f_s/(2f_B)$. What is the value of f_B for a 14 bit analog-to-digital converter using this modulator if the sampling frequency, f_s, is 10MHz?



Solution

$$Y(z) = Q(z) + \frac{1}{1+z^{-2}}[X(z) + z^{-2}Y(z)] = Q(z) + \frac{X(z)}{1+z^{-2}} + \frac{z^{-2}Y(z)}{1+z^{-2}} \rightarrow Y(z) = (1+z^{-2})Q(z) + X(z)$$

$$N(z) = Y(z)\Big|_{X(z)=0} = (1+z^{-2})Q(z) \qquad \rightarrow \qquad N(f) = N(e^{j\omega T}) = (1 + e^{-2\omega T})Q(f)$$

$$N(f) = \frac{e^{j\omega T}}{e^{j\omega T}}(1 + e^{-2\omega T})Q(f) = \frac{e^{j\omega T} + e^{-j\omega T}}{e^{j\omega T}}Q(f) = \frac{2\cos(\omega T)}{e^{j\omega T}}\frac{\Delta}{\sqrt{6f_s}} = \frac{4\Delta}{\sqrt{6f_s}}\cos(\omega T)\, e^{-j\omega T}$$

$$n_o^2(f) = \int_{f_1}^{f_2}|N(f)|^2 df = \int_{f_1}^{f_2}\frac{4\Delta^2}{6f_s}\cos^2(\omega T)df = \frac{\Delta^2}{3f_s}\int_{f_1}^{f_2}[1+\cos(2\omega T)]df$$

$$= \frac{\Delta^2}{3f_s}\int_{f_1}^{f_2} df + \frac{\Delta^2}{3f_s}\int_{f_1}^{f_2}\cos\left(\frac{4\pi f}{f_s}\right)df = \frac{\Delta^2}{3f_s}(f_2-f_1) + \frac{\Delta^2}{3f_s}\left[\frac{f_s}{4\pi}\sin\left(\frac{4\pi f}{f_s}\right)\right]_{f_1}^{f_2}$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[\sin\left(\frac{4\pi f_2}{f_s}\right) - \sin\left(\frac{4\pi f_1}{f_s}\right)\right]$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[2\cos\left(\frac{2\pi}{f_s}(f_2+f_1)\right)\sin\left(\frac{2\pi}{f_s}(f_2-f_1)\right)\right] = \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[\cos\left(\frac{4\pi f_o}{f_s}\right)\sin\left(\frac{2\pi f_B}{f_s}\right)\right]$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[\cos(\pi)\sin\left(\frac{2\pi f_B}{f_s}\right)\right] = \frac{\Delta^2}{3f_s}f_B - \frac{\Delta^2}{12\pi}\left[\sin\left(\frac{2\pi f_B}{f_s}\right)\right]$$

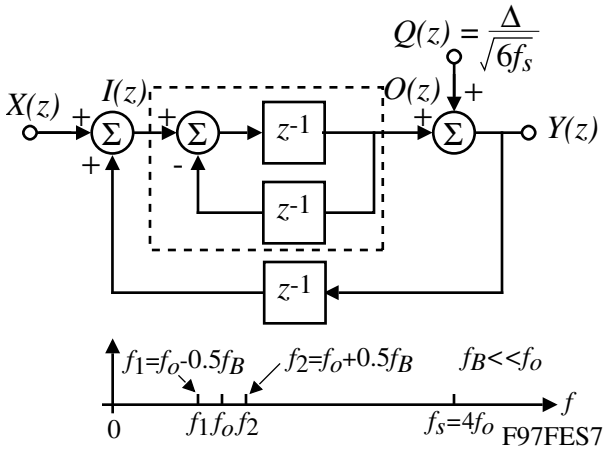
$$n_o^2(f) \approx \frac{\Delta^2}{3f_s}f_B - \frac{\Delta^2}{12\pi}\left[\frac{2\pi f_B}{f_s} - \frac{1}{6}\left(\frac{2\pi f_B}{f_s}\right)^2 + \cdots\right] \approx \frac{\Delta^2}{3f_s}f_B - \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2\pi}{36}\left(\frac{2f_B}{f_s}\right)^2$$

$$n_o^2(f) = \frac{\Delta^2\pi}{36}\left(\frac{2f_B}{f_s}\right)^2 \rightarrow \quad n_o(f) = \frac{\Delta\sqrt{\pi}}{6}\left(\frac{2f_B}{f_s}\right) \le \frac{\Delta}{2^{14}}$$

$$\therefore \quad \frac{2f_B}{f_s} \le \left(\frac{6}{2^{14}\sqrt{\pi}}\right)^{2/3} = 0.003095 \quad \Rightarrow \quad f_B \le \frac{0.003095}{2}\text{x}10\text{MHz} = \underline{\underline{15.47\text{kHz}}}$$

Problem 10.9-10

A first-order, 1-bit, bandpass, delta-sigma modulator is shown. Find the modulation noise spectral density, $N(f)$, and integrate the square of the magnitude of $N(f)$ over the bandwidth of interest (f_1 to f_2) and find an expression for the noise power, $n_o(f)$, in the bandwidth of interest in terms of Δ and the oversampling factor M where $M = f_s/(2f_B)$. What is the value of f_B for a 12 bit analog-to-digital converter using this modulator if the sampling frequency, f_s, is 100MHz? Assume that $f_s=4f_o$ and $f_B<<f_o$.



Solution

To find the noise transfer function, set $X(z) = 0$ and solve for $Y(z)$. The transfer function for the dashed box is

$$O(z) = z^{-1}[I(z) - z^{-1}O(z)] \;\rightarrow\; \frac{O(z)}{I(z)} = \frac{z^{-1}}{1-z^{-2}} \quad \therefore \; Y(z) = Q(z) + \frac{z^{-2}}{1+z^{-2}}Y(z)$$

or $$Y(z)\left[1 - \frac{z^{-2}}{1+z^{-2}}\right] = Q(z) \;\Rightarrow\; Y(z)[1+z^{-2}-z^{-2}] = [1+z^{-2}]Q(z) \;\Rightarrow\; Y(z) = [1+z^{-2}]Q(z)$$

$$\therefore \quad N(z) = (1+z^{-2})Q(z) \;\rightarrow\; N(\varepsilon^{j\omega T}) = (1+e^{-j2\omega T})Q(f) = \frac{e^{j\omega T}+e^{-j\omega T}}{e^{j\omega T}}Q(f)$$

Substituting for $Q(f)$ gives $N(f) = \dfrac{2\Delta}{\sqrt{6f_s}}\cos(\omega T)\, e^{-j\omega T}$

$$n_o^2(f) = \int_{f_2}^{f_1}|N(f)|^2 df = \int_{f_2}^{f_1}\frac{4\Delta}{6f_s}\cos^2(\omega T)\, e^{-j\omega T}\, df = \frac{\Delta^2}{3f_s}\int_{f_2}^{f_1}[1+\cos 2\omega T]df$$

$$= \frac{\Delta^2}{3f_s}\int_{f_2}^{f_1}df + \frac{\Delta^2}{3f_s}\int_{f_2}^{f_1}\cos\left(\frac{4\pi f}{f_s}\right)df = \frac{\Delta^2}{3f_s}(f_2-f_1) + \frac{\Delta^2}{12\pi}\left[\sin\left(\frac{4\pi f_2}{f_s}\right) - \sin\left(\frac{4\pi f_1}{f_s}\right)\right]$$

$$= \frac{\Delta^2}{3f_s}f_B + \frac{\Delta^2}{12\pi}\left[2\cos\left(\frac{4\pi}{f_s}\right)\left(\frac{f_2+f_1}{2}\right)\sin\left(\frac{2\pi}{f_s}\right)(f_2-f_1)\right] = \frac{\Delta^2 f_B}{3f_s} + \frac{\Delta^2}{6\pi}\left[\cos\left(\frac{4\pi f_o}{f_s}\right)\sin\left(\frac{2\pi f_B}{f_s}\right)\right]$$

$$\therefore \; n_o^2(f) \approx \frac{\Delta^2 f_B}{3f_s} - \frac{\Delta^2}{6\pi}\left[\frac{2\pi f_B}{f_s} - \frac{1}{6}\left(\frac{2\pi f_B}{f_s}\right)+\cdots\right] \Rightarrow \boxed{n_o^2(f) = \frac{\Delta^2\pi^2}{36}\left(\frac{2f_B}{f_s}\right)^3 = \left(\frac{\Delta\pi}{6}\right)^2\frac{1}{M^3}}$$

$$n_o(f) = \frac{\Delta\pi}{6}\frac{1}{M^{3/2}} \le \frac{\Delta}{2^{13}} \;\rightarrow\; \frac{2f_B}{f_s} \le \left(\frac{6}{2^{13}\pi}\right)^{2/3} = 0.006013 \;\rightarrow\; \boxed{f_B \le 189\text{kHz}}$$