Introduction to IC

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Outline

- The IC History
- Moor's Law
- Manufacturing Process
- What is ASIC
- Classification of ASIC
- Design Flow Introduction

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Transistor Revolution

- Transistor –Bardeen (Bell Labs) in 1947
- Bipolar transistor – Schockley in 1949
- First bipolar digital logic gate – Harris in 1956
- First monolithic IC – Jack Kilby in 1959
- First commercial IC logic gates – Fairchild 1960
- TTL – 1962 into the 1990's
- ECL – 1974 into the 1980's

MOSFET Technology

- MOSFET transistor - Lilienfeld (Canada) in 1925 and Heil (England) in 1935
- CMOS – 1960's, but plagued with manufacturing problems
- PMOS in 1960's (calculators)
- NMOS in 1970's (4004, 8080) – for speed
- CMOS in 1980's – preferred MOSFET technology because of power benefits
- BiCMOS, Gallium-Arsenide, Silicon-Germanium
- SOI (silicon-on-insulator), Copper-Low K, …

Birth of Modern Electronics -- 1947

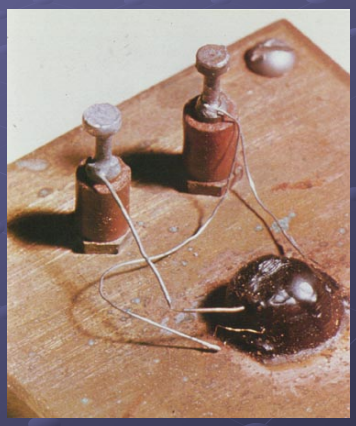
AT&T Bell Laboratories -- Invention of Point Contact Transistor
William Shockley, Walter Brittain, and John Bardeen
Winners of the 1956 Nobel Prize in Physics

Vacuum tubes ruled in first half of 20th century: Large, expensive, power-hungry, unreliable

But now, everything changes!

Solid-State Electronics Goes Commercial -- 1950

AT&T Bell Laboratories -- Junction Transistor

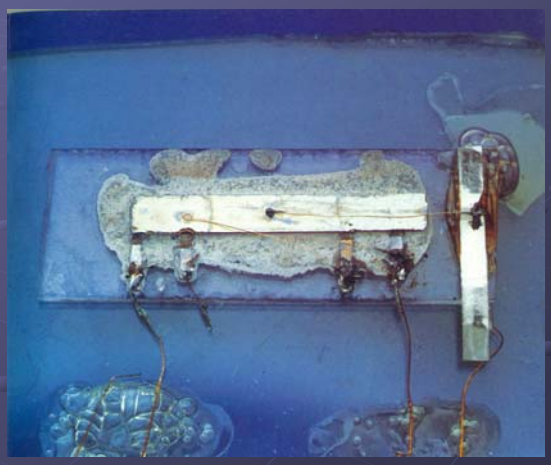


Microelectronic Revolution -- 1958

The First Integrated Circuit –- Jack Kilby, Texas Instruments

1 Transistor and 4 Other Devices on one Chip

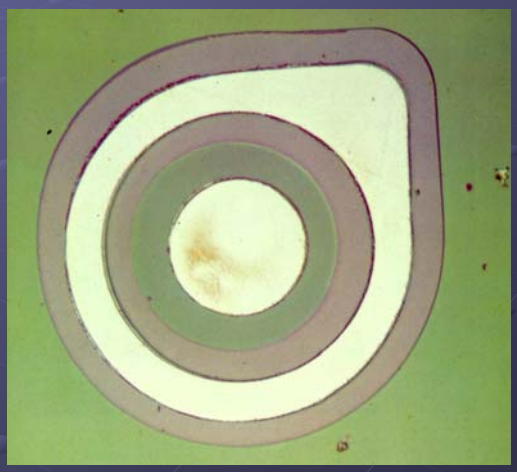
Winner of the 2000 Nobel Prize



The Planar Process -- 1959

A More Efficient Way to Make Transistors

Fairchild Electronics -- Jean Hoerni and Robert Noyce

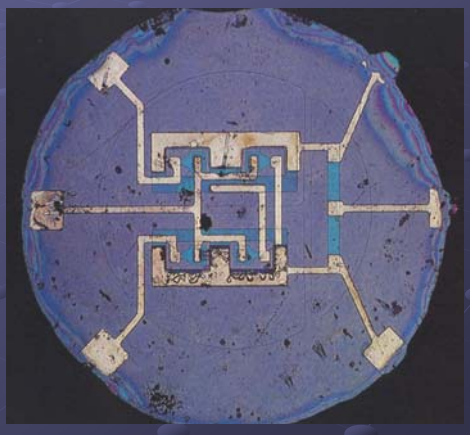


First Commercial Planar IC

Fairchild -- One Binary Digital (Bit) Memory Device on a Chip

4 Transistors and 5 Resistors

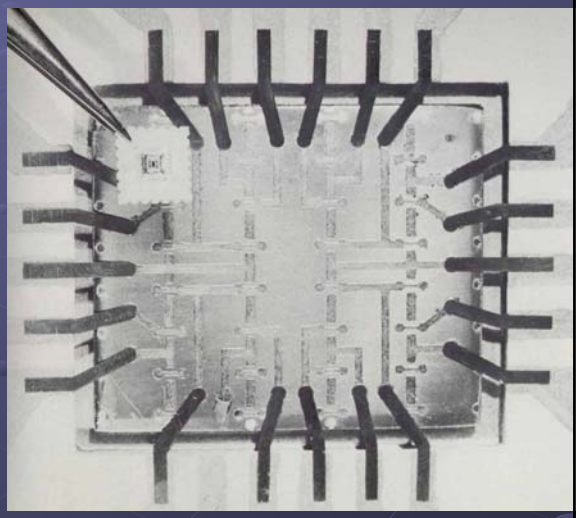
Start of SSI Technology



A New Form of Transistor -- 1962

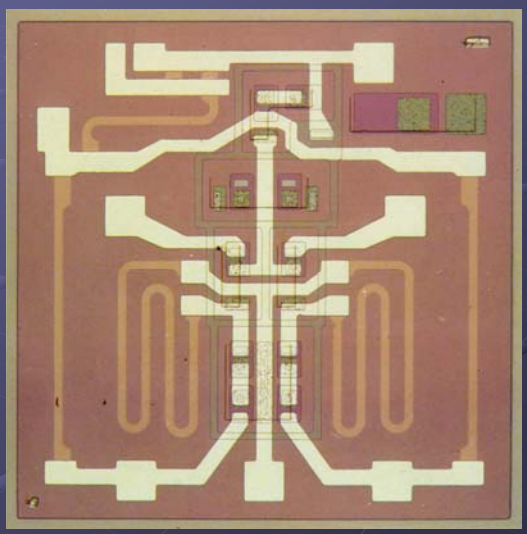
Metal-Oxide Semiconductor Field-Effect Transistor (MOSFET)

Radio Corporation of America (RCA) Sarnoff Laboratories



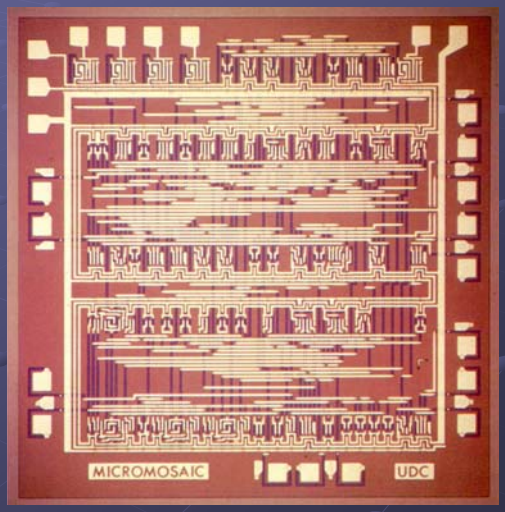
First Linear IC -- 1964

The μA 702 OPAMP – Fairchild



First IC Created with CAD -- 1967

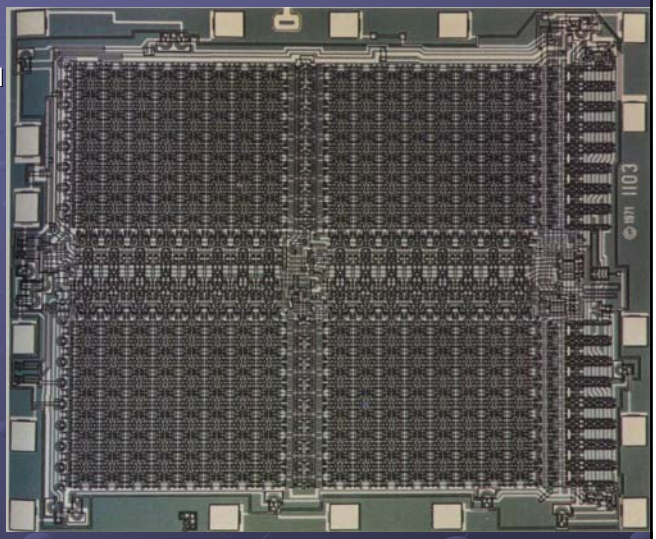
μMOSAIC – Fairchild



First 1,024 Bit Memory Chip -- 1970

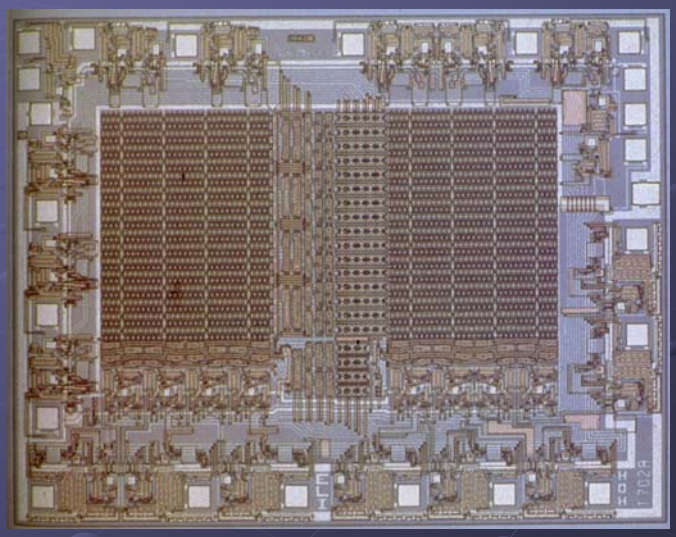
Intel Corporation DRAM

- 1970's processes usually had only nMOS transistors
  - *Inexpensive, but consume power while idle*
- 1980s-present: CMOS processes for low idle power



First EPROM -- 1971

The INTEL 1702



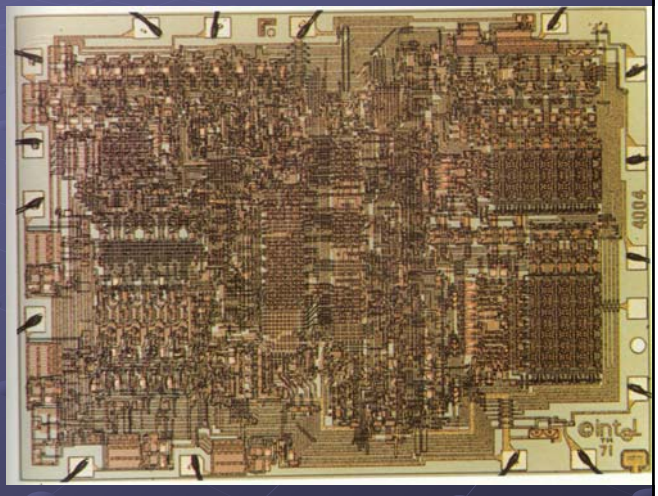
Birth of the Microprocessor -- 1971

The Intel 4004 – 2,300 Transistors

THE FIRST COMPUTER ON A SINGLE CHIP,

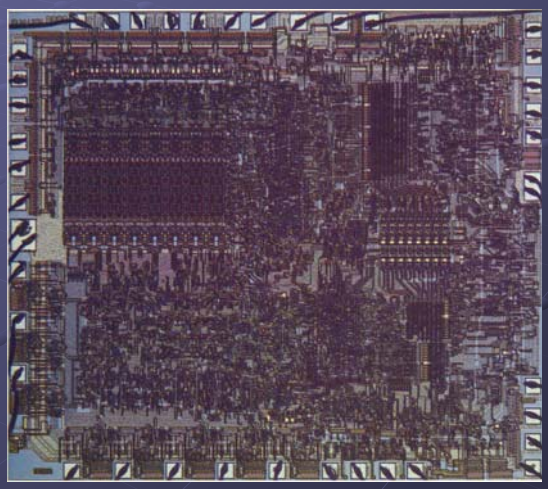
Beginning of LSI Technology

10um process, 108KHz



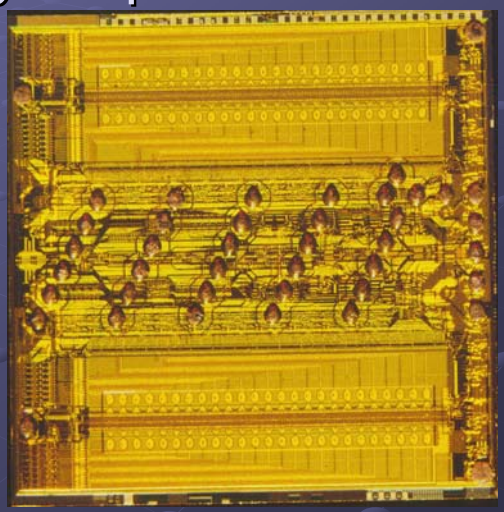
First General-Purpose Microprocessor -- 1974

8-Bit Intel 8080, Intel Corporation – 4,500 Transistors



First 65,536 Bit Dynamic Memory Chip -- 1977

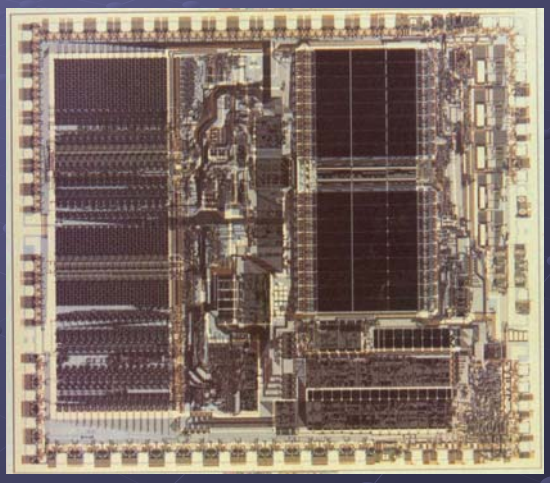
IBM Corporation



One of the Most Powerful 16-Bit Microprocessors -- 1979

The Motorola 68000

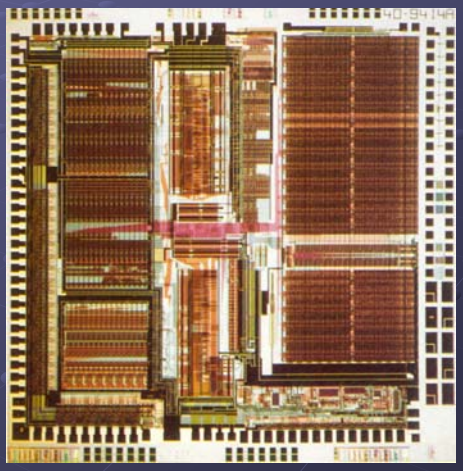
WELL INTO THE LSI ERA



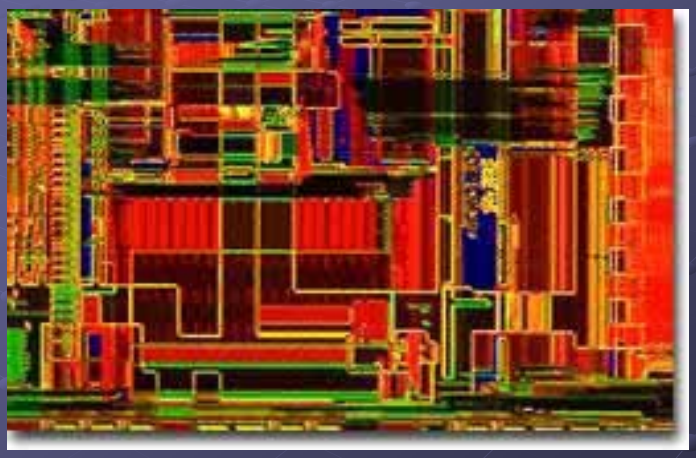
A Very Early 32-Bit Microprocessor -- 1981

The HP Focus Chip, Hewlett-Packard Co. – 450,000 Transistors

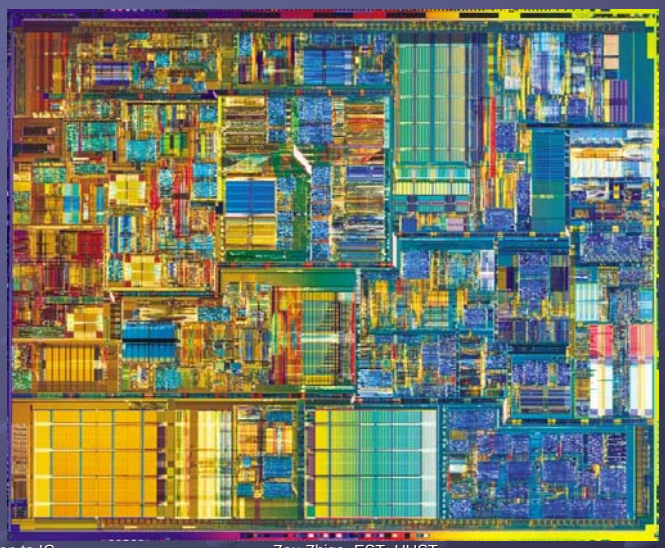
THE VLSI ERA BEGINS



Intel Pentium μProcessor – 1993 --3 million transistors



Intel Pentium 4 μProcessor – 2003 --55 million transistors



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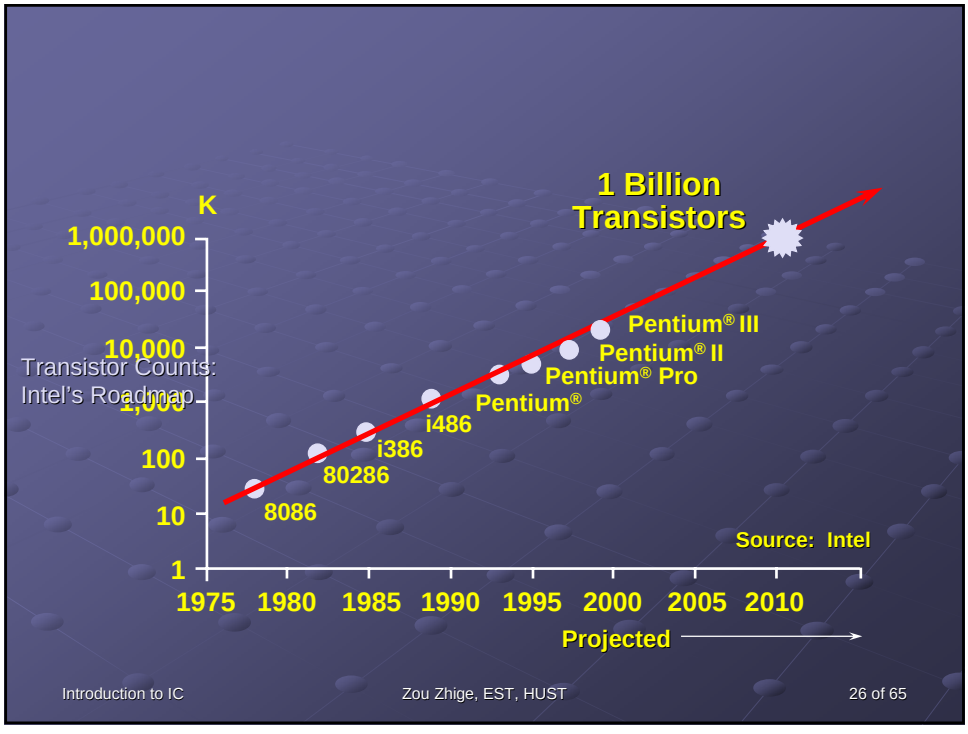
Moore's Law

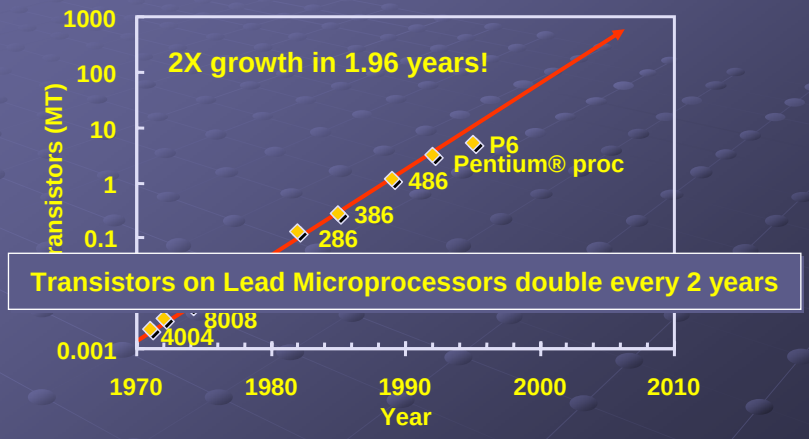
- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months.

Transistor Counts: Intel's Roadmap

Intel's CPU	Year of introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™ processor	1985	275,000
486™ DX processor	1989	1,180,000
Pentium® processor	1993	3,100,000
Pentium II processor	1997	7,500,000
Pentium III processor	1999	24,000,000
Pentium 4 processor	2000	42,000,000

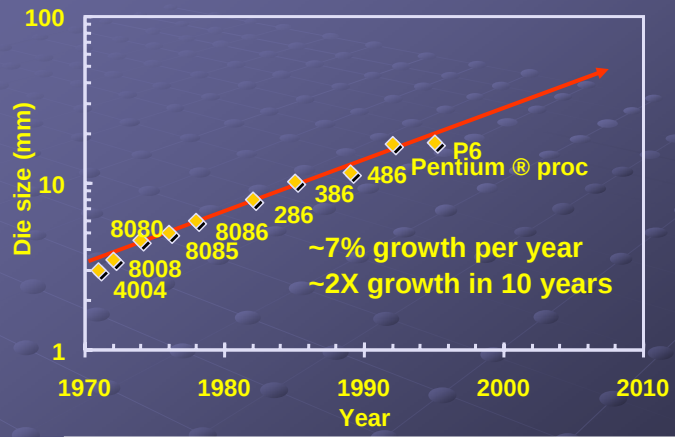


Moore's law in Microprocessors



Transistors on Lead Microprocessors double every 2 years

Die Size Growth



Die size grows by 14% to satisfy Moore's Law

Frequency

Lead Microprocessors frequency doubles every 2 years

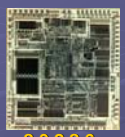
Power Dissipation

Lead Microprocessors power continues to increase

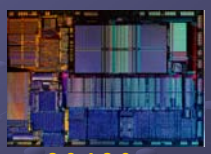
Intel microprocessor Roadmap


8080

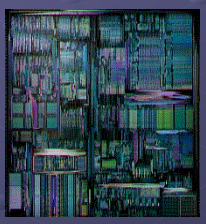

8086

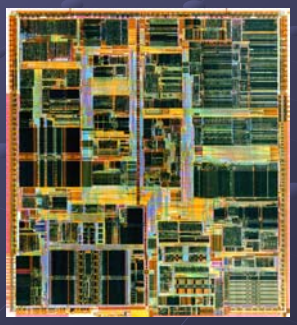

80286


80386


80486


Pentium


PentiumPro


Pentium (IV)

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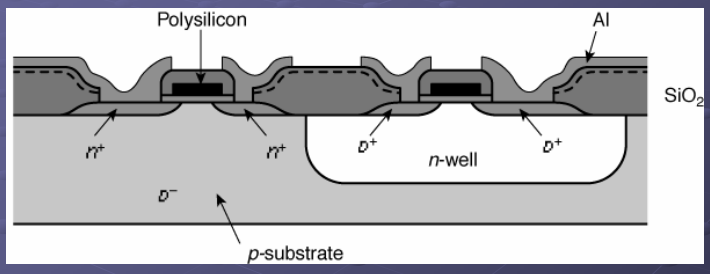
Manufacturing Process

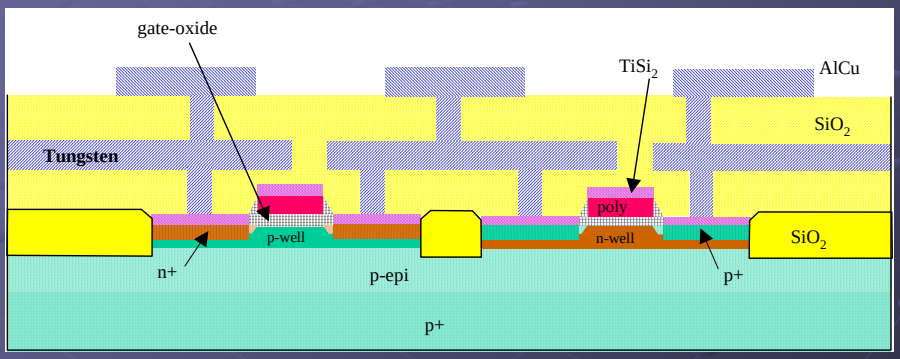
- CMOS Process
- Photo-Lithographic Process
- Packaging

CMOS Process



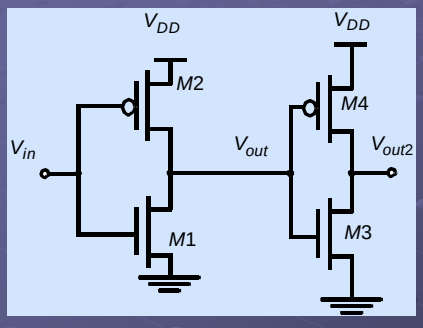
Basic Process: P-Sub N-well

A Modern CMOS Process



Dual-Well CMOS Process

Circuit Under Design



Its Layout View

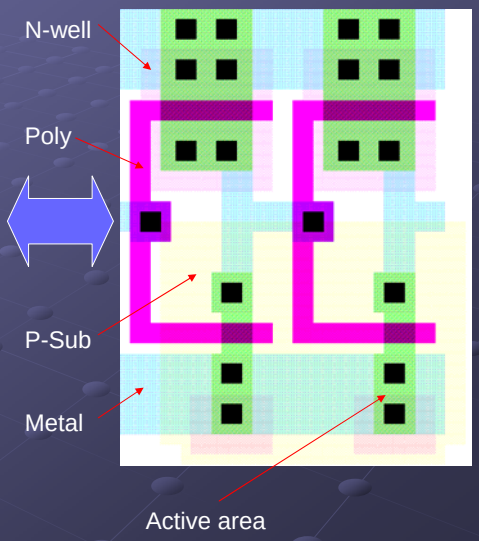
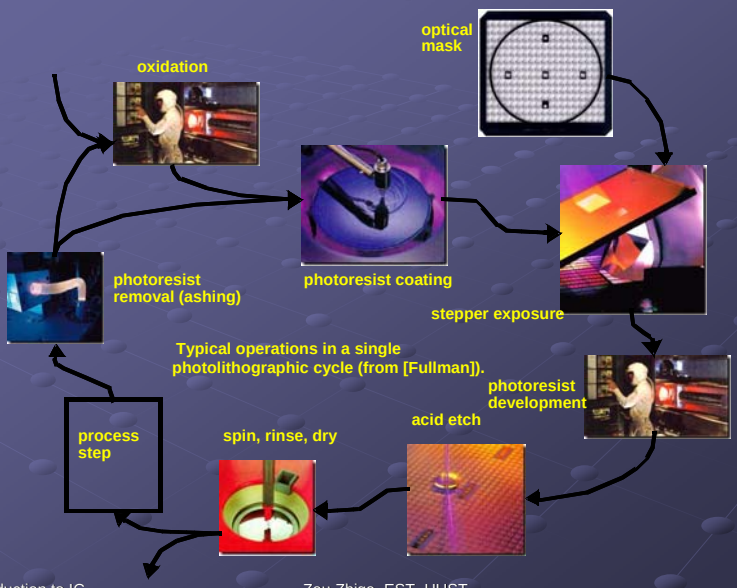
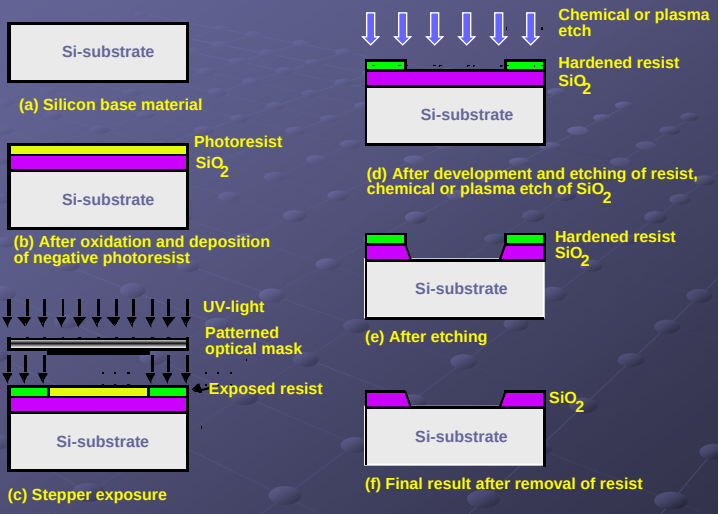


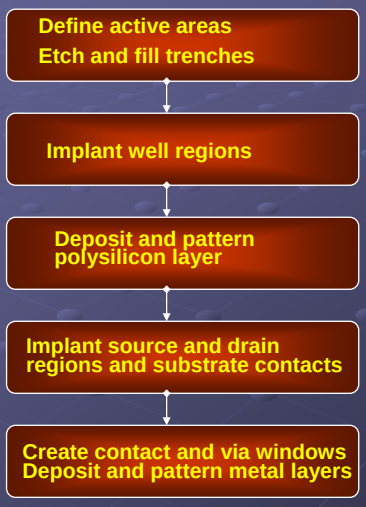
Photo-Lithographic Process



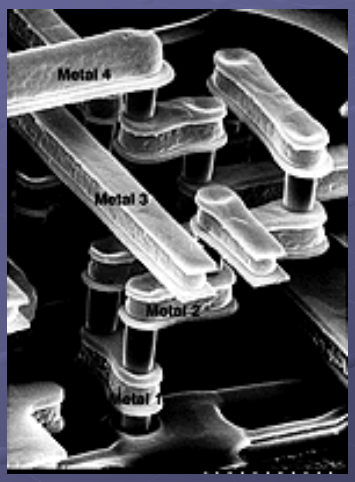
Patterning of SiO_2

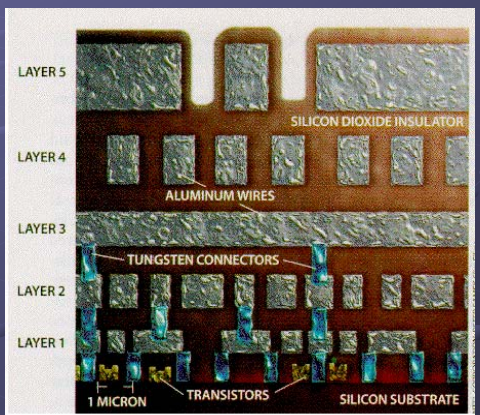


CMOS Process at a Glance



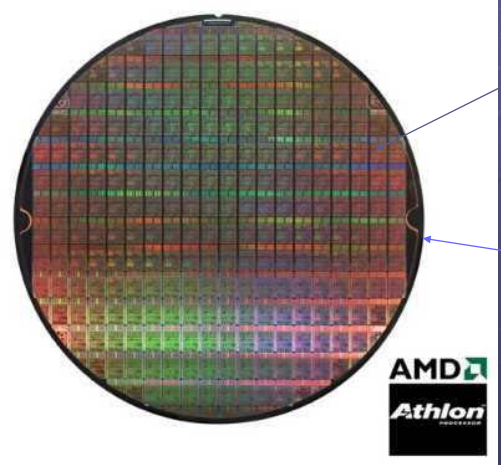
Advanced Metallization





5-layer cross-section of chip

Wafer → Die



Single die

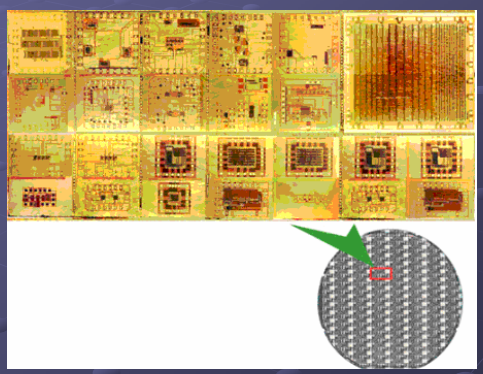
Wafer

Going up to 12″ (30cm)

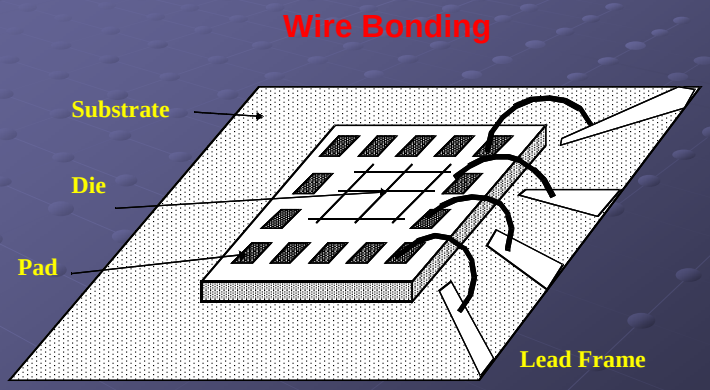
From http://www.amd.com

Multi Project Wafer(MPW)

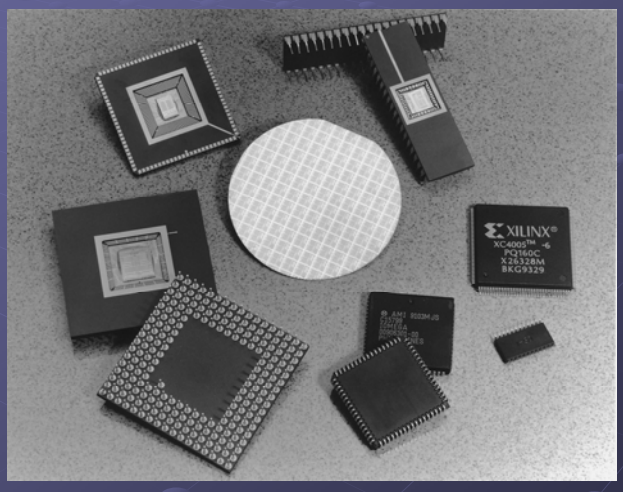
- Low price
- Schedule
- Testing



Packaging : Bonding Techniques



Package Types



Surface Mount Device Package

- **BGA:** Ball Grid Array
- **BQFP:** Bumpered Quad Flat Pack
- **CBGA:** Ceramic Ball Grid Array
- **CFP:** Ceramic Flat Pack
- **CPGA:** Ceramic Pin Grid Array
- **CQFP:** Ceramic Quad Flat Pack
- **TBD:** Ceramic Lead-Less Chip Carrier
- **DLCC:** Dual Lead-Less Chip Carrier (Ceramic)
- **FBGA:** Fine-pitch Ball Grid Array
- **fpBGA:** Fine Pitch Ball Grid Array
- **JLCC:** J-Leaded Chip Carrier (Ceramic)
- **LCC:** Leaded Chip Carrier
- **LCCC:** Leaded Ceramic Chip Carrier
- **PLCC:** Plastic Leaded Chip Carrier
- **PQFD:** ----
- **PQFP:** Plastic Quad Flat Pack
- **PSOP:** Plastic Small-Outline Package
- **QSOP:** Quarter Size Outline Package
- **SOIC:** Small Outline IC
- **SSOP:** Shrink Small-Outline Package
- **TQFP:** Thin Quad Flat Pack
- **TSOP:** Thin Small-Outline Package
- **TSSOP:** Thin Shrink Small-Outline Package
- **TVSOP:** Thin Very Small-Outline Package
- **VQFB:** Very-thin Quad Flat Pack

Through Hole Device Package

- **CERDIP:** Ceramic DIP
- **DIP:** Dual In-line Package
- **TBD:** Dual In-line Zig-Zag Package
- **HDIP:** Hermetic DIP
- **PDIP:** Plastic DIP
- **PGA:** Pin Grid Array
- **SIP:** Single In-line Package

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ASIC Definition

Application-Specific Integrated Circuit: a chip designed for a particular application (as opposed to the general application) by defining the interconnection of a set of basic circuit building blocks drawn from a library provided by the circuit manufacturer.

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ASIC Classification 1

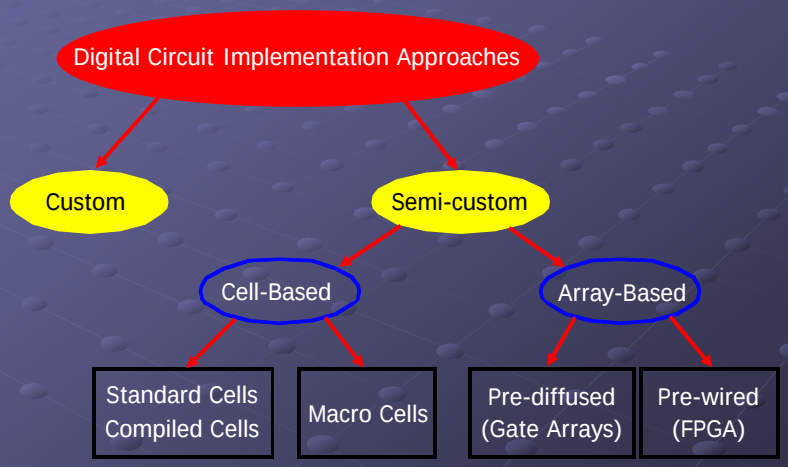
1. General Purpose IC

   (8051, 74L138, 74161, 8255, 555, CPU)

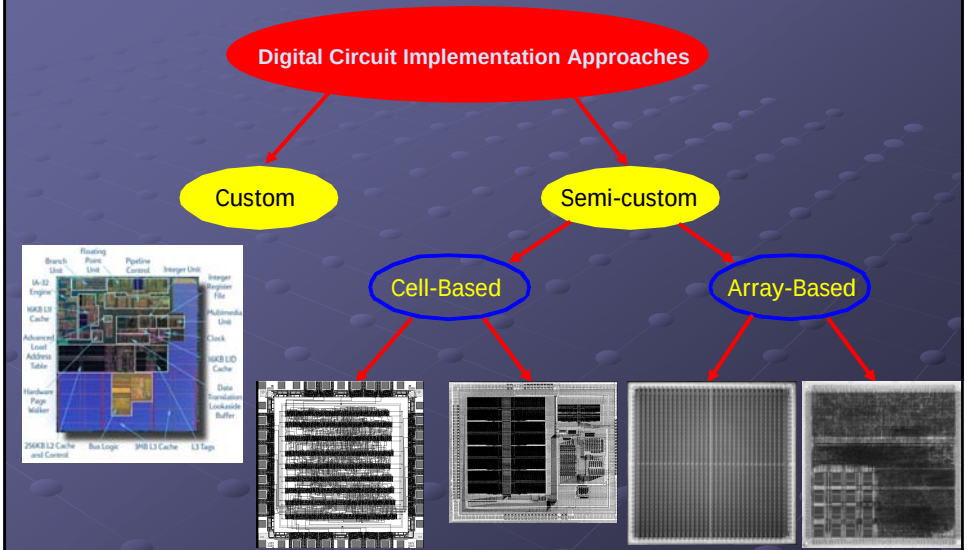
2. Application-Specific Integrated Circuit

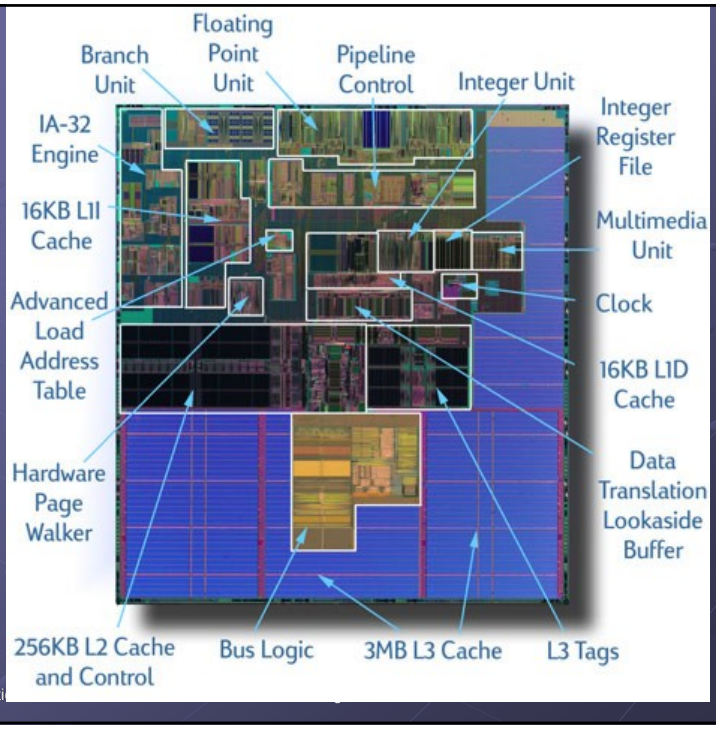
   (Our design aim: LCD driver and controller, real time clock, DVD, MP3, USB2.0, Power Management, IC card, MEMS)

ASIC Classification 2



Implementation methodologies





Glossary

- Full Custom
  - Designed at the transistor level. Every transistor is optimized
  - Custom packages
  - Highly process technology-dependent
- Standard-Cell
  - Designed at the gate (cell) level
  - Cell library is pre-characterized
  - all cells have fixed height
  - wiring may be restricted to channels

Glossary

- Gate Array
  - Like Standard-cell
  - transistors prefabricated; customize metal to generate cells
- FPGA
  - Like Gate-Array
  - Logic blocks are programmable
  - Interconnect is programmable
  - chips prefabricated

Remember: full-custom ASICs

- All mask layers are customized
- Make sense only if there are no libraries
- **Advantages**
  - **the highest performance** **fast, low power**
  - **the lowest part cost** **smallest die size**
- **Disadvantages**
  - **increased design time**
  - **complexity**
  - **design expense**
  - **highest risk**
- Microprocessors **were exclusively** full-custom

Full-Custom Application

- Memory
- CPU and communication IC
- Analog and Mix-signal IC

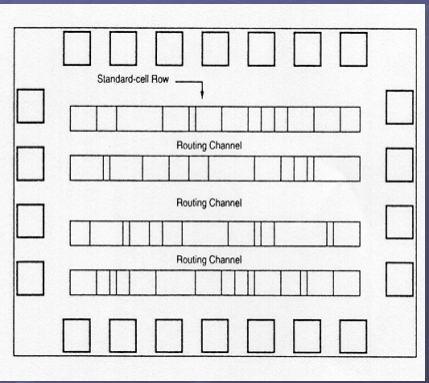
- Price, Performance, Market

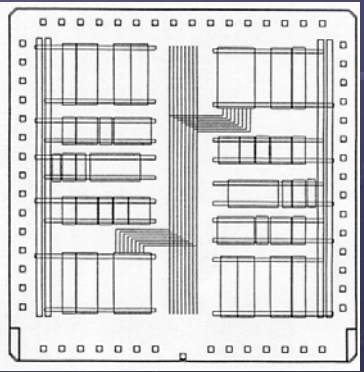
Stand Cell

概念：从标准单元库中调用事先经过精心设计的逻辑单元，排列成行，行间留有可调整的布线通道，再按功能要求将各内部单元以及输入/输出单元连接起来，形成所需的专用电路。

芯片布局：芯片中心是单元区，输入/输出单元和压焊块在芯片四周，基本单元具有等高不等宽的结构，布线通道区没有宽度的限制，利于实现优化布线。

标准单元





标准单元法与门阵列法比较

SC法设计流程与GA法相似，但有若干基本的不同点：

(1) 在门阵列法中逻辑图是转换成门阵列所具有的单元或宏单元，而标准单元法则转换成标准单元库中所具有的标准单元。

(2) 门阵列设计时首先要选定某一种门复杂度的基片，因而门阵列的布局和布线是在最大的门数目、最大的压焊块数目、布线通道的间距都确定的前提下进行的。标准单元法则不同，它的单元数、压焊块数取决于具体设计的要求，而且布线通道的间距是可变的，当布线发生困难时，通道间距可以随时加大，因而布局和布线是在一种不太受约束的条件下进行的。

(3) 门阵列设计时只需要定制部分掩膜版，而标准单元设计后需要定制所有的各层掩膜版。

标准单元法与门阵列法相比的优点：

(1) 芯片面积的利用率比门阵列法要高。芯片中没有无用的单元，也没有无用的晶体管。

(2) 可以保证100％的连续布通率。

(3) 单元能根据设计要求临时加以特殊设计并加入库内，因而可得到较佳的电路性能。

(4) 可以与全定制设计法相结合。在芯片内放入经编译得到的宏单元或人工设计的功能块。

标准单元法也存在不足：

(1) 原始投资大：单元库的开发需要投入大量的人力物力；当工艺变化时，单元的修改工作需要付出相当大的代价，因而如何建立一个在比较长的时间内能适应技术发展的单元库是一个突出问题。

(2) 成本较高：由于掩膜版需要全部定制，芯片的加工也要经过全过程，因而成本较高。只有芯片产量达到某一定额(几万至十几万)，其成本才可接受。

ASIC Classification 3

Chip classification according to number of active elements

classification	# transistors	example
SSI	1 - 100	gates
MSI	100 - 1k	registers
LSI	1k - 100k	uP
VLSI	100K -1M	RAM, sig. proc
ULSI	1M -	?

ASIC Classification 4

From the Function of IC

- Analog IC
- Digital IC
- Mix-Signal IC

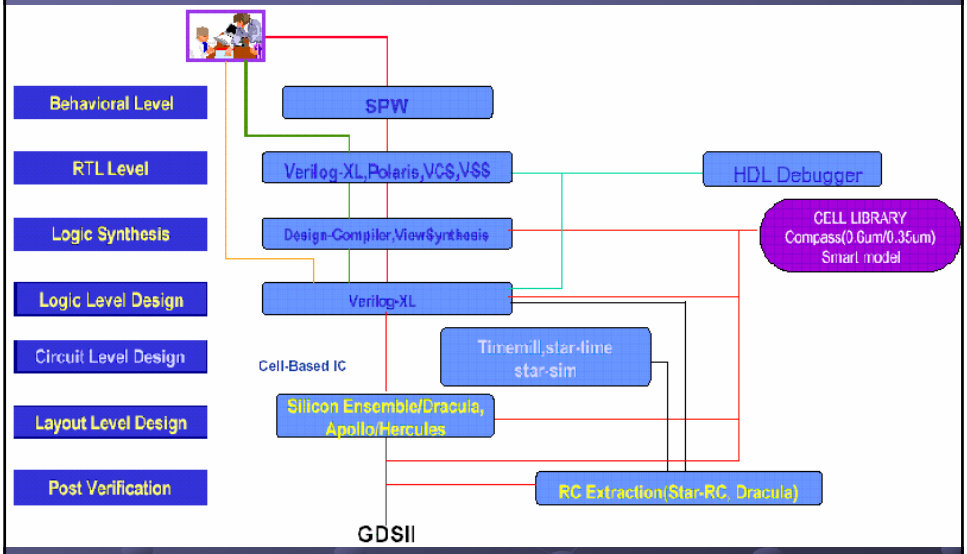
Outline

- The IC History
- Moor's Law
- Manufacturing Process
- What is ASIC
- Classification of ASIC
- ASIC Design Flow Introduction

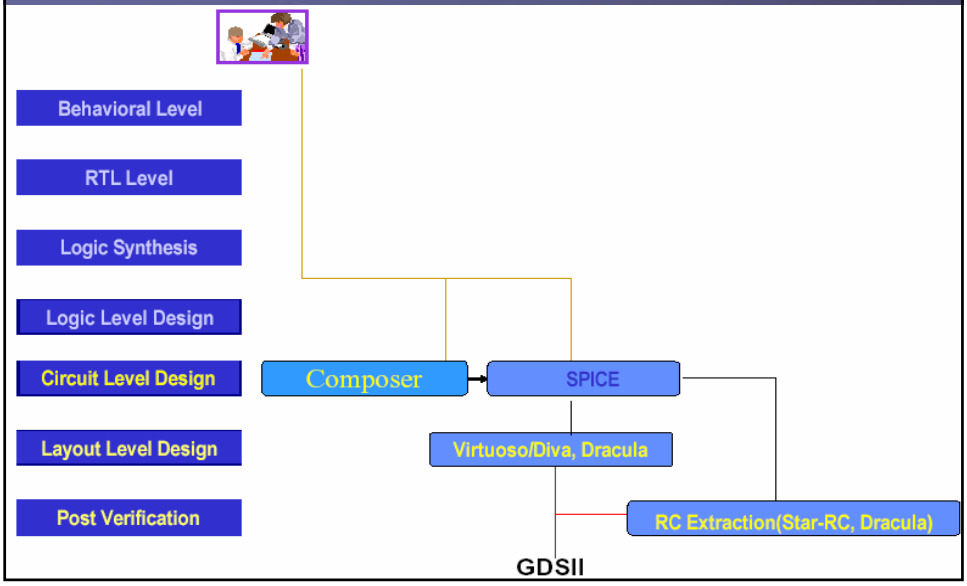
ASIC Design Flow

- Cell Based IC
- Full Custom IC
- Mix-Signal IC

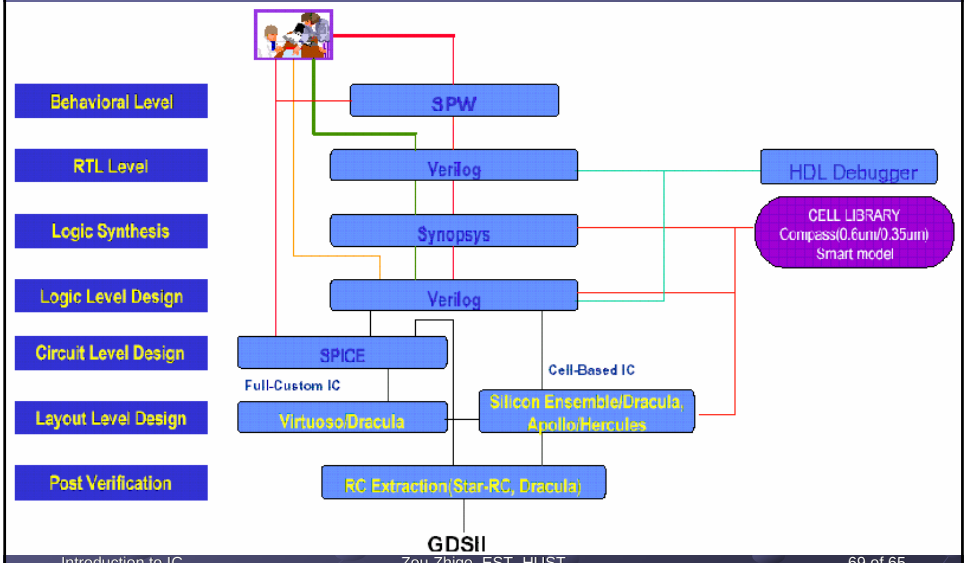
Cell Based Design Flow

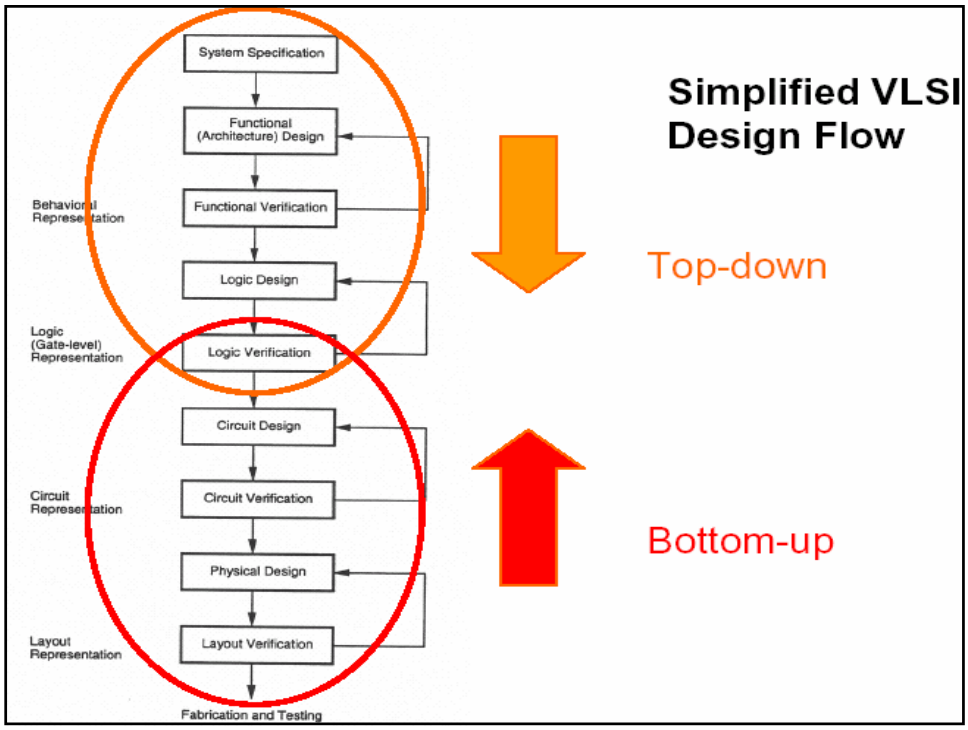


Full Custom Design Flow



Mix-Signal Design Flow





Glossary

- IDM—Fabless—Foundry—Chipless
- Wafer, die
- EDA tools
- MPW
- IP (Intelligence Property)
- SPEC (specification)
- “the chain” in economy: 1~2: 10: 100
- Front End: Coding, Simulation, Synthesis.
- Back End: Layout
- Top Down: Digital
- Bottom Up: Analog

Q & A

Thanks !